SONY

Diagonal 11.016mm (Type 2/3) Progressive Scan CCD Image Sensor for B/W Cameras

ICX625ALA

Description

The ICX625ALA is a diagonal 11.016mm (Type 2/3) interline CCD solid-state image sensor with a square pixel array and 5.05M effective pixels. Progressive scan enables all pixel signals to be output separately within approximately 1/15 second, and also output using various addition and elimination methods. This chip features an electronic shutter with variable charge-storage time which makes it possible to realize full-frame still images without a mechanical shutter. High sensitivity and low dark current are achieved through the adoption of Super HAD CCD technology.

Features

- ◆ High horizontal and vertical resolution
- ◆ Supports following readout modes
  - All-pixel scan mode (15 frames/s)
  - 4/16-line readout mode
  - Center scan mode
- ◆ Square pixel
- ◆ Horizontal drive frequency: 60.0MHz
- ◆ No reset gate bias voltage adjustment
- ◆ Substrate bias applied from external method
- ◆ High sensitivity, low dark current, excellent antiblooming characteristics
- ◆ Continuous variable-speed shutter function
- ◆ 28-pin high-precision plastic package

Package

28-pin DIP (Plastic)

Super HAD CCD™

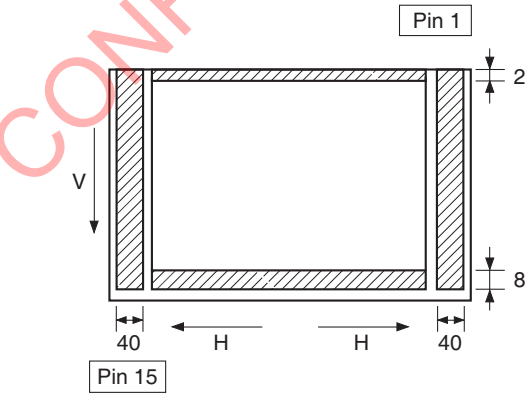
* Super HAD CCD is a trademark of Sony Corporation. The Super HAD CCD is a version of Sony's high performance CCD HAD (Hole-Accumulation Diode) sensor with sharply improved sensitivity by the incorporation of a new semiconductor technology developed by Sony Corporation.

Device Structure

- ◆ Interline CCD image sensor
- ◆ Image size
  Diagonal 11.016mm (Type 2/3)
- ◆ Total number of pixels
  2536 (H) × 2068 (V) approx. 5.24M pixels
- ◆ Number of effective pixels
  2456 (H) × 2058 (V) approx. 5.05M pixels
- ◆ Number of active pixels
  2448 (H) × 2050 (V) approx. 5.02M pixels
- ◆ Chip size
  9.93mm (H) × 8.70mm (V)
- ◆ Unit cell size
  3.45μm (H) × 3.45μm (V)
- ◆ Optical black
  Horizontal (H) direction: front 40 pixels (per channel)
  Vertical (V) direction: front 8 pixels, rear 2 pixels
- ◆ Number of dummy bits
  Horizontal: front 1 (per channel)
  Vertical: 1
- ◆ Substrate material
  Silicon

Optical Black Position

(Top View)



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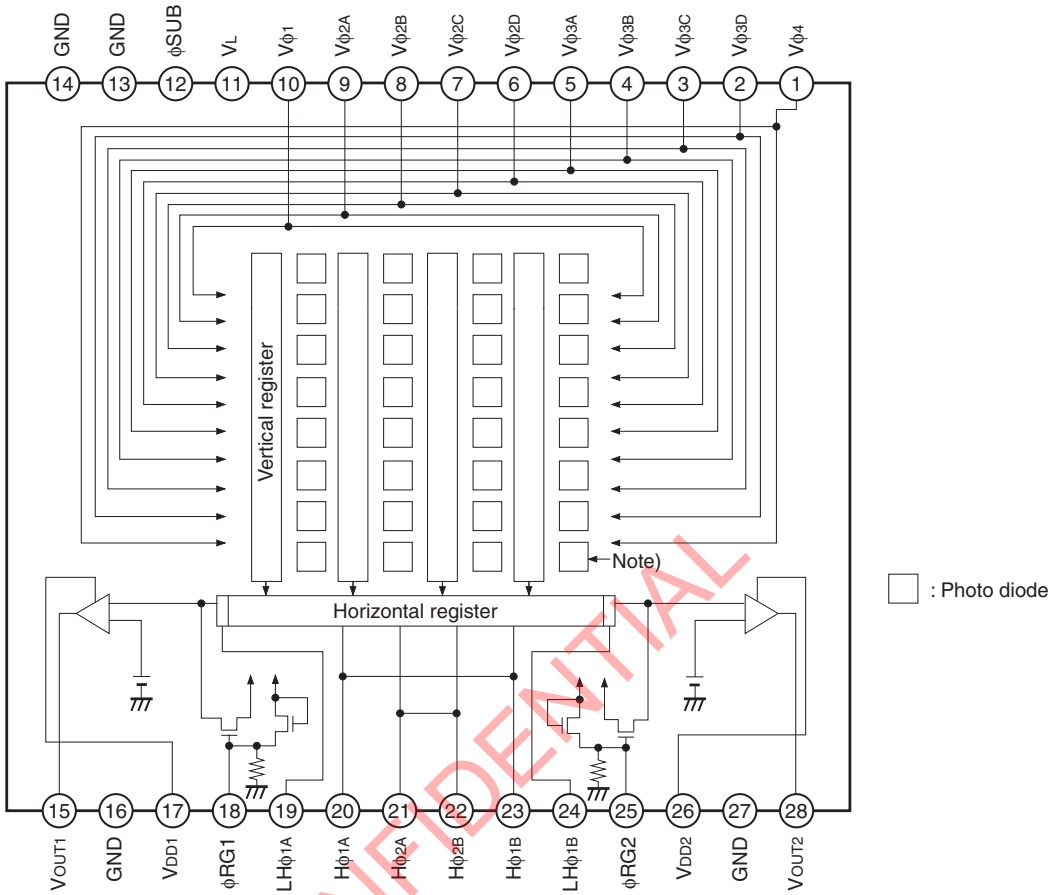
Block Diagram and Pin Configuration

(Top View)



Pin Description

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	Vφ4	Vertical register transfer clock	15	VOUT1	Signal output 1
2	Vφ3D	Vertical register transfer clock	16	GND	GND
3	Vφ3C	Vertical register transfer clock	17	VDD1	Supply voltage 1
4	Vφ3B	Vertical register transfer clock	18	φRG1	Reset gate clock
5	Vφ3A	Vertical register transfer clock	19	LHφ1A	Horizontal register final stage transfer clock
6	Vφ2D	Vertical register transfer clock	20	Hφ1A	Horizontal register transfer clock
7	Vφ2C	Vertical register transfer clock	21	Hφ2A	Horizontal register transfer clock
8	Vφ2B	Vertical register transfer clock	22	Hφ2B	Horizontal register transfer clock
9	Vφ2A	Vertical register transfer clock	23	Hφ1B	Horizontal register transfer clock
10	Vφ1	Vertical register transfer clock	24	LHφ1B	Horizontal register final stage transfer clock
11	VL	Protective transistor bias	25	φRG2	Reset gate clock
12	φSUB	Substrate clock	26	VDD2	Supply voltage 2
13	GND	GND	27	GND	GND
14	GND	GND	28	VOUT2	Signal output 2

Absolute Maximum Ratings

Item		Ratings	Unit	Remarks
Against φSUB	V_{DD1}, V_{DD2}, V_{OUT1}, V_{OUT2}, φRG1, φRG2 – φSUB	–40 to +12	V	
	$V\phi 2\alpha$, $V\phi 3\alpha$ – φSUB (α = A to D)	–50 to +15	V	
	$V\phi 1$, $V\phi 4$, V_L – φSUB	–50 to +0.3	V	
	$LH\phi 1\beta$, $H\phi 1\beta$, $H\phi 2\beta$, GND – φSUB (β = A, B)	–40 to +0.3	V	
Against GND	V_{DD1}, V_{DD2}, V_{OUT1}, V_{OUT2}, φRG1, φRG2 – GND	–0.3 to +22	V	
	$V\phi 1$, $V\phi 2\alpha$, $V\phi 3\alpha$, $V\phi 4$ – GND (α = A to D)	–10 to +18	V	
	$LH\phi 1\beta$, $H\phi 1\beta$, $H\phi 2\beta$ – GND (β = A, B)	–10 to +6.5	V	
Against V_L	$V\phi 2\alpha$, $V\phi 3\alpha$ – V_L (α = A to D)	–0.3 to +28	V	
	$V\phi 1$, $V\phi 4$, $H\phi 1\beta$, $H\phi 2\beta$, GND – V_L (β = A, B)	–0.3 to +15	V	
Between input clock pins	Potential difference between vertical clock input pins	to +15	V	*1
	$H\phi 1\beta$ – $H\phi 2\beta$ (β = A, B)	–6.5 to +6.5	V	
	$LH\phi 1\beta$, $H\phi 1\beta$, $H\phi 2\beta$ – $V\phi 4$ (β = A, B)	–10 to +16	V	
Storage temperature		–30 to +80	°C	
Performance guarantee temperature		–10 to +60	°C	
Operating temperature		–10 to +75	°C	*2

*1 Guaranteed up to 24V when the clock width < 10μs and the clock duty factor < 0.1%.

*2 This product generates more heat compared to other Sony CCD products due to its specifications.
Be sure to thoroughly take radiation countermeasure and then use the product with the temperature of the bottom of the package in the operating temperature range.

Bias Conditions

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply voltage	V_{DD}	14.55	15.0	15.45	V	
Protective transistor bias	V_L		*1		V	
Substrate voltage adjustment range	V_{SUB}	7.8		13.4	V	*2
Substrate voltage adjustment precision	ΔV_{SUB}	Indicated voltage – 0.2	Indicated voltage	Indicated voltage + 0.2	V	*2
Reset gate clock	ϕRG1, ϕRG2		*3			

*1 For the V_L setting, use the V_{VL} voltage of the vertical clock waveform or the same voltage as the V_L power supply of the V driver.

*2 The setting value of the substrate voltage (V_{SUB}) is marked on the back of the image sensor by a code. Adjust the substrate voltage to the indicated voltage externally. The adjustment precision is ±0.2V.

*3 Do not apply a DC bias to the reset gate clock pin, because a DC bias is generated internally.

V_{SUB} code - 1-digit indication □

↑

V_{SUB} code

The codes and the actual values correspond as follows.

V_{SUB} code	1	2	3	4	6	7	8	9	A	C	d	E	f	G	h
Actual value	7.8	8.0	8.2	8.4	8.6	8.8	9.0	9.2	9.4	9.6	9.8	10.0	10.2	10.4	10.6

V_{SUB} code	J	K	L	m	N	P	R	S	U	V	W	X	Y	Z
Actual value	10.8	11.0	11.2	11.4	11.6	11.8	12.0	12.2	12.4	12.6	12.8	13.0	13.2	13.4

[Example] "h" → V_{SUB} = 10.6V setting

DC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply current	I_{DD}		19.0		mA	*1

*1 Connect the constant current source shown in the drive circuit example to V_{OUT1} and V_{OUT2}.

Clock Voltage Conditions

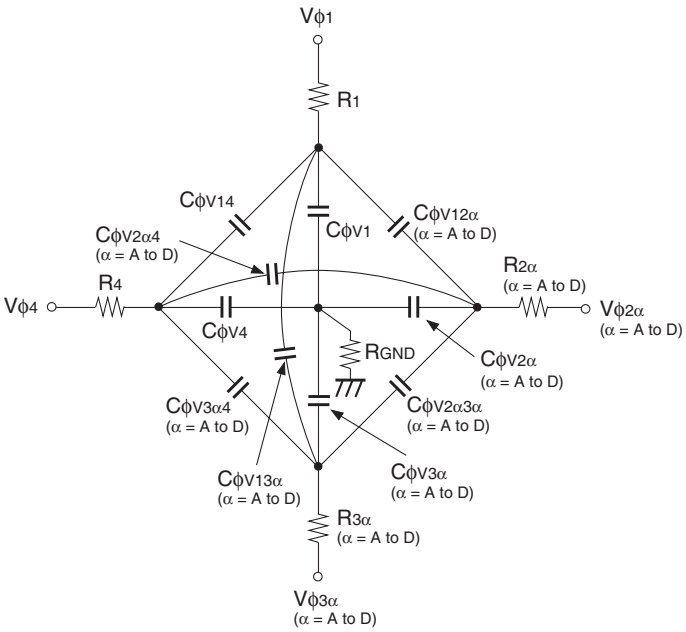
Item	Symbol	Min.	Typ.	Max.	Unit	Waveform diagram	Remarks
Readout clock voltage	V_{VT}	14.55	15.0	15.45	V	1	
Vertical transfer clock voltage	V_{VH1}, V_{VH2}	–0.05	0	0.05	V	2	$V_{VH} = (V_{VH1} + V_{VH2})/2$
	V_{VH3}, V_{VH4}	–0.2	0	0.05	V	2	
	V_{VL1}, V_{VL2}, V_{VL3}, V_{VL4}	–8.3	–8.0	–7.7	V	2	$V_{VL} = (V_{VL3} + V_{VL4})/2$
	$V_{\phi V}$	7.5	8.0	8.35	V	2	$V_{\phi V} = V_{VHn} – V_{VLn}$ (n = 1 to 4)
	$V_{VH3} – V_{VH}$	–0.25		0.1	V	2	
	$V_{VH4} – V_{VH}$	–0.25		0.1	V	2	
	V_{VHH}			0.9	V	2	High-level coupling
	V_{VHL}			0.9	V	2	High-level coupling
	V_{VLH}			0.9	V	2	Low-level coupling
	V_{VLL}			0.7	V	2	Low-level coupling
Horizontal transfer clock voltage	$V_{\phi H}$	3.4	3.6	3.8	V	3	
	V_{HL}	–0.05	0	0.05	V	3	
	V_{CR}	$V_{\phi H}/2$			V	3	Cross-point voltage
Reset gate clock voltage	$V_{\phi RG}$	3.4	3.6	3.8	V	4	
	$V_{RGLH} – V_{RGLL}$			0.4	V	4	Low-level coupling
	$V_{RGL} – V_{RGLm}$			0.5	V	4	Low-level coupling
Substrate clock voltage	$V_{\phi SUB}$	22.2	23.0	23.8	V	5	

Clock Equivalent Circuit Constants

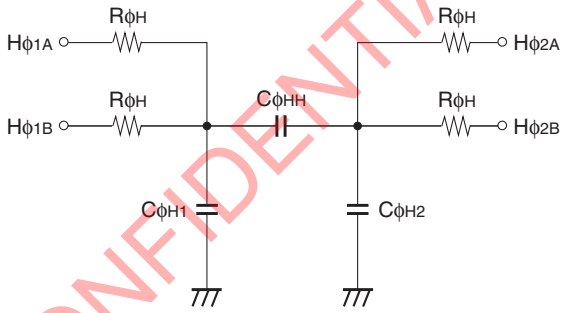
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Capacitance between vertical transfer clock and GND	$C_{\phi V1}$		5620		pF	
	$C_{\phi V2A}$, $C_{\phi V2B}$, $C_{\phi V2C}$, $C_{\phi V2D}$		3320		pF	
	$C_{\phi V3A}$, $C_{\phi V3B}$, $C_{\phi V3C}$, $C_{\phi V3D}$		3320		pF	
	$C_{\phi V4}$		5620		pF	
Capacitance between vertical transfer clocks	$C_{\phi V12\ (A, B, C, D)}$		680		pF	
	$C_{\phi V13\ (A, B, C, D)}$		680		pF	
	$C_{\phi V14}$		15000		pF	
	$C_{\phi V2\ (A, B, C, D),\ 3\ (A, B, C, D)}$		100		pF	
	$C_{\phi V2\ (A, B, C, D),\ 4}$		220		pF	
	$C_{\phi V3\ (A, B, C, D),\ 4}$		680		pF	
Capacitance between horizontal transfer clock and GND	$C_{\phi H1}$		82		pF	
	$C_{\phi H2}$		56		pF	
Capacitance between horizontal transfer clocks	$C_{\phi HH}$		30		pF	
Capacitance between reset gate clock and GND	$C_{\phi RG}$		2		pF	
Capacitance between horizontal final stage transfer clock and GND	$C_{\phi LH1}$		4		pF	
Capacitance between substrate clock and GND	$C_{\phi SUB}$		1500		pF	
Vertical transfer clock series resistance	R_1		56		Ω	
	$R_{2\ (A, B, C, D)}$		62		Ω	
	$R_{3\ (A, B, C, D)}$		68		Ω	
	R_4		30		Ω	
Vertical transfer clock ground resistance	R_{GND}		16		Ω	
Horizontal transfer clock series resistance	$R_{\phi H}$		4.3		Ω	
Reset gate clock series resistance	$R_{\phi RG1}$		2.2		Ω	

Note) 1. Expressions using parentheses such as $C_{\phi V12\ (A, B, C, D)}$ indicate items which include all combinations of the pins within the parentheses.
For example, $C_{\phi V12\ (A, B, C, D)}$ indicates $C_{\phi V12A}$, $C_{\phi V12B}$, $C_{\phi V12C}$ and $C_{\phi V12D}$.

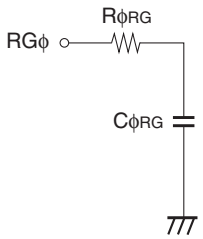
2. $C_{\phi V2\alpha 2\beta}$ and $C_{\phi V3\alpha 3\beta}$ (α = A to D, β = A to D except α) are sufficiently small relative to other capacitance between vertical transfer clocks in the equivalent circuit, and are also below the measurement limit, so these are omitted from the equivalent circuit diagrams.



Vertical transfer clock equivalent circuit



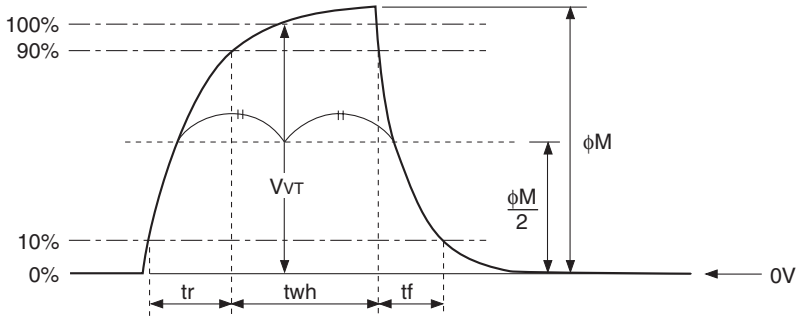
Horizontal transfer clock equivalent circuit



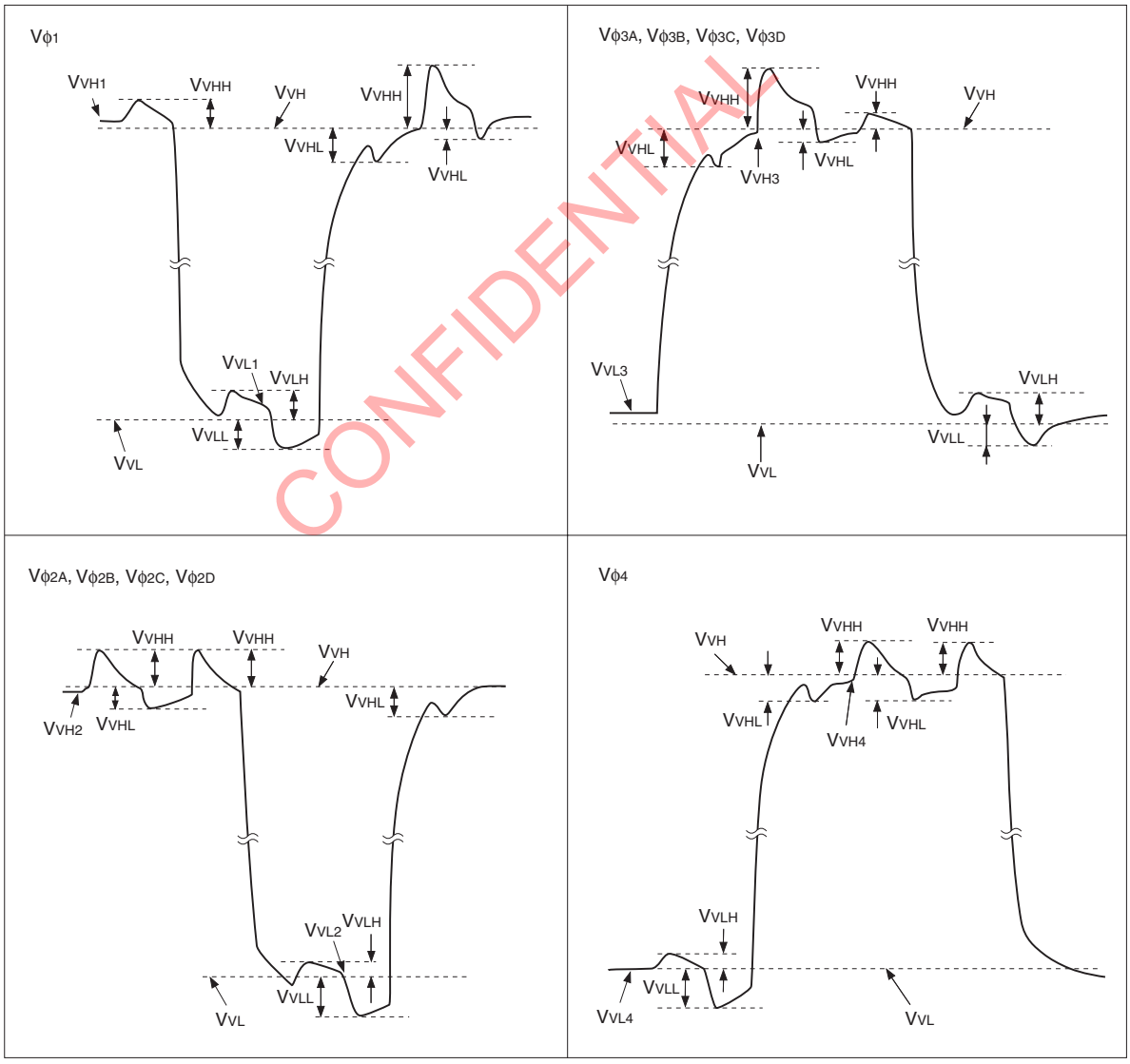
Reset gate clock equivalent circuit

Drive Clock Waveform Conditions

1. Readout clock waveform

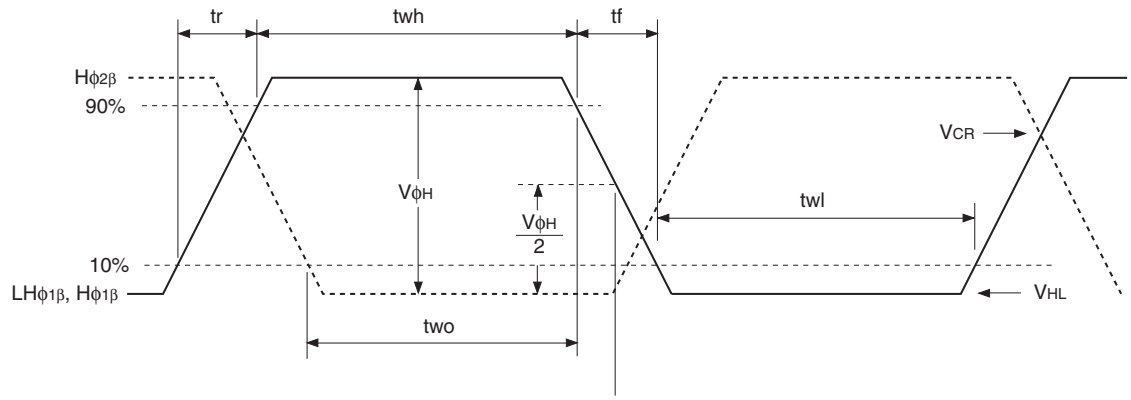


2. Vertical transfer clock waveform



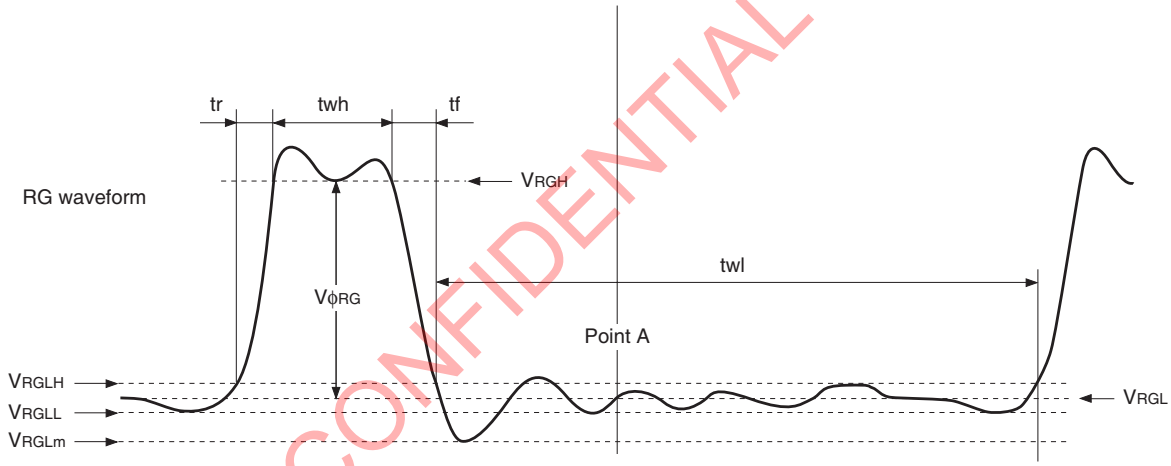
$V_{VH} = (V_{VH1} + V_{VH2})/2$
$V_{VL} = (V_{VL3} + V_{VL4})/2$
$V_{\phi V} = V_{VHn} - V_{VLn}$ (n = 1 to 4)

3. Horizontal transfer clock waveform



VCR is the cross-point voltage of the horizontal transfer clocks LHϕ1β, Hϕ1β and Hϕ2β waveforms that is on the Hϕ1β rise side.
"two" is the overlapped period with twh and twl of the horizontal transfer clocks LHϕ1β, Hϕ1β and Hϕ2β. (β = A, B)

4. Reset gate clock waveform



VRGLH is the maximum value and VRGLL is the minimum value of the coupling waveform during the period from Point A in the above diagram until the rising edge of RG.
In addition, VRGL is the average value of VRGLH and VRGLL.

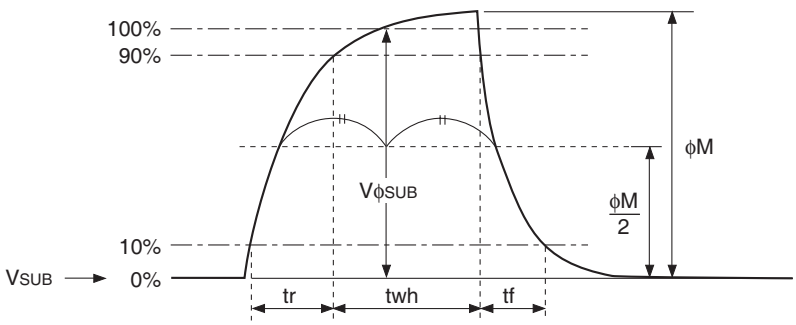
$$V_{RGL} = (V_{RGLH} + V_{RGLL})/2$$

Assuming VRGH is the minimum value during the interval twh, then;

$$V_{\phi RG} = V_{RGH} - V_{RGL}$$

VRGLm is the negative overshoot level during the falling edge of RG.

5. Substrate clock waveform



Clock Switching Characteristics

(Horizontal drive frequency: 60.0MHz)

Item	Symbol	twh			twl			tr			tf			Unit	Remarks
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Readout clock	V_T	8.13	8.33						0.5			0.5		μs	During readout
Vertical transfer clock	$V\phi1$, $V\phi4$, $V\phi2\alpha$, $V\phi3\alpha$ (α = A to D)										15		250	ns	When using CXD3400N
Horizontal transfer clock	$H\phi1\beta$ (β = A, B)	4.5	5		4.5	5			3	3.5		3	3.5	ns	When driving at 3.4V during imaging, tf ≥ tr – 2ns
	$H\phi2\beta$ (β = A, B)	4.5	5		4.5	5			3	3.5		3	3.5		
Horizontal final stage transfer clock	$LH\phi1\beta$ (β = A, B)		6.5			6.5			1.5			1.5		ns	
Reset gate clock	ϕRG	2.5	3.0			10.0			1.5			1.5		ns	
Substrate clock	ϕSUB	1.3	1.35							0.5			0.5	μs	When draining charge

Item	Symbol	two			Unit	Remarks
		Min.	Typ.	Max.		
Horizontal transfer clock	$H\phi1A$, $H\phi1B$, $H\phi2A$, $H\phi2B$	4.5	5		ns	

Spectral Sensitivity Characteristics

(excludes lens characteristics and light source characteristics)

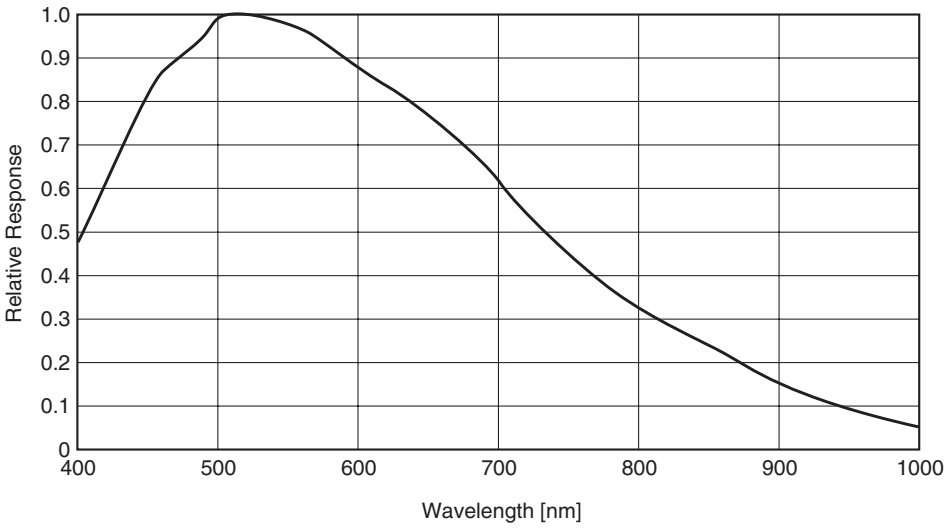


Image Sensor Characteristics

(Ta = 25℃)

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement method	Remarks
Sensitivity	S	330	420		mV	1	1/30s accumulation
Saturation signal	Vsat	360			mV	2	Ta = 60℃
Smear	Sm		–95	–90	dB	3	All-pixel scan mode*1
			–83	–78			4/16-line readout mode
Video signal shading	SH			20	%	4	Zone 0 and I
				25			Zone 0 to II'
Dark signal	Vdt			4	mV	5	Ta = 60℃, 15 frame/s
Dark signal shading	ΔVdt			2	mV	6	Ta = 60℃, 15 frame/s, *2
Lag	Lag			0.5	%	7	

The maximum difference of the output signals between right and left output (Vout1, Vout2) is 10%.

*1 Same for center scan mode.

*2 Excludes vertical dark signal shading caused by vertical register high-speed transfer.

Zone Definition of Video Signal Shading

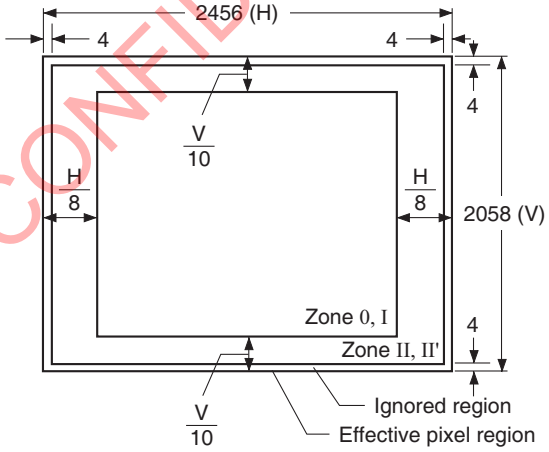


Image Sensor Characteristics Measurement Method

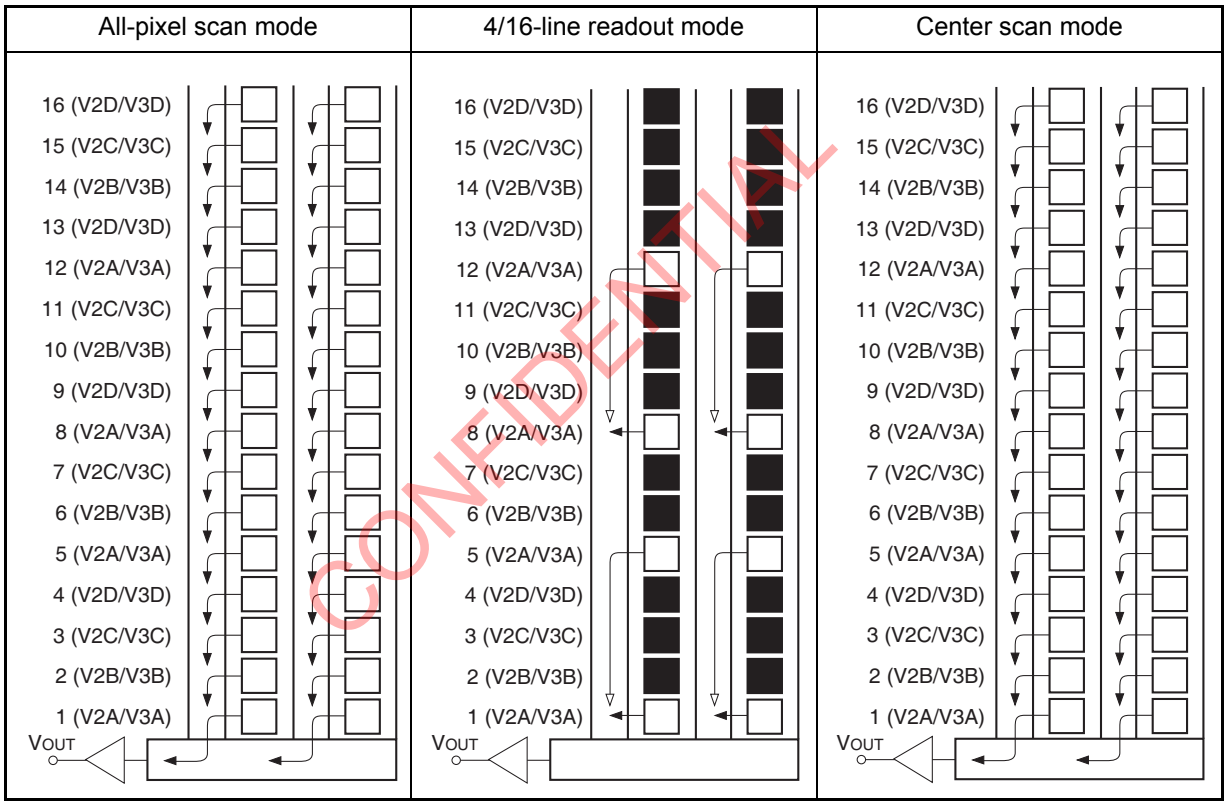
Readout modes list

The readout method, frame rate, number of output lines and other information for each readout mode are shown in the table below.

Mode	Readout method	Addition method	Frame rate [frame/s]	Number of output lines of effective image data
All-pixel scan	All-pixel scan	None	15.0	2058
4/16-line readout	4/16-line readout	Vertical 2-line	37.54	257
Center scan	All-pixel scan	None	18.04 to 43.74	1600 to 246

Description of Readout Mode

The output methods for the following three readout modes are shown below.



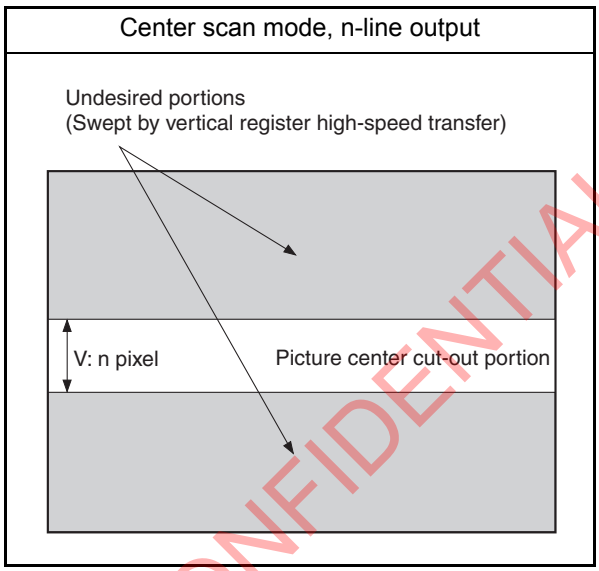
Note) Blacked out portions in the diagram indicate pixels which are not read out.

1. All-pixel scan mode
   In this mode, all pixel signals are output in non-interlace format in 1/15s.
   All pixel signals within the same exposure period are read out simultaneously, making this mode suitable for high resolution image capturing.

2. 4/16-line readout mode
   By reading out signals of four lines (1st, 5th, 8th and 12th line) for every 16 lines and adding two pixels in the horizontal register, all effective area signals are output at higher frame rate than all-pixel scan mode.
   The number of output lines is 257.

Description of Operation in Center Scan Mode

The center scan mode realizes high frame rates by sweeping the top and bottom of the picture with high-speed transfer and cutting out the center of the picture.



n = 246, 480, 720, 960, 1200, 1600

Measurement conditions

1. In the following measurements, the device drive conditions are at the typical values of the bias and clock voltage conditions.
2. In the following measurements, spot pixels are excluded and, unless otherwise specified, the optical black (OB) level is used as the reference for the signal output, which is measured at point [*A] in Drive Circuit.

Definition of standard imaging conditions

◆ Standard imaging condition I:
Use a pattern box (luminance: 706cd/m^2, color temperature of 3200K halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t = 1.0mm) as an IR cut filter and image at F8. The luminous intensity to the sensor receiving surface at this point is defined as the standard sensitivity testing luminous intensity.

◆ Standard imaging condition II:
Image a light source (color temperature of 3200K) with a uniformity of brightness within 2% at all angles. Use a testing standard lens with CM500S (t = 1.0mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

1. Sensitivity
Set the measurement condition to the standard imaging condition I. After setting the electronic shutter mode with a shutter speed of 1/100s, measure the signal output (Vs) at the center of the screen, and substitute the value into the following formula.

$$S = Vs \times (100/30)$$

2. Saturation signal
Set the measurement condition to the standard imaging condition II. After adjusting the luminous intensity to 10 times the intensity with the average value of the signal output, 150mV, measure the minimum value of the signal.

3. Smear
Set the measurement condition to the standard imaging condition II. With the lens diaphragm at F5.6 to F8, adjust the luminous intensity to 500 times the intensity with the average value of the signal output, 150mV. When the readout clock is stopped and the charge drain is executed by the electronic shutter at the respective H blankings, measure the maximum value of the signal output (VSm), and substitute the value into the following formula.

$$Sm = 20 \times \log \{(VSm/150mV) \times (1/500) \times (1/10)\} \text{ [dB] (1/10V method conversion value)}$$

4. Video signal shading
Set the measurement condition to the standard imaging condition II. With the lens diaphragm at F5.6 to F8, adjust the luminous intensity so that the average value of the signal output is 150mV. Then measure the maximum value (Vmax) and the minimum value (Vmin) of the signal output, and substitute the values into the following formula.

$$SH = (Vmax - Vmin)/150mV \times 100 \text{ [\%]}$$

5. Dark signal
Measure the average value of the signal output (Vdt) with the device ambient temperature 60℃ and the device in the light-obstructed state using the horizontal idle transfer level as a reference.

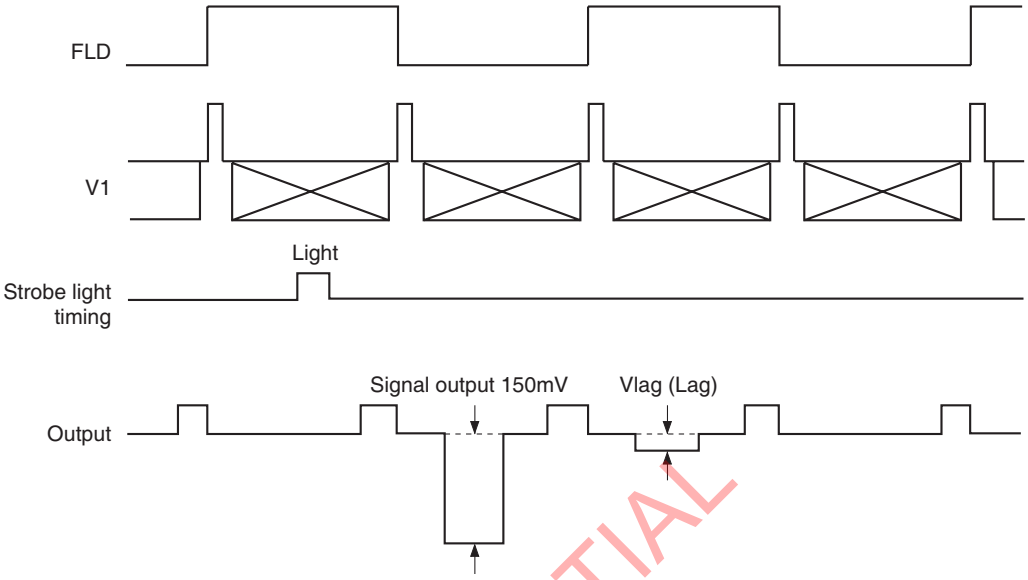
6. Dark signal shading
After the measurement item 5, measure the maximum value (Vdmax) and the minimum value (Vdmin) of the dark signal output, and substitute the values into the following formula.

$$\Delta Vdt = Vdmax - Vdmin$$

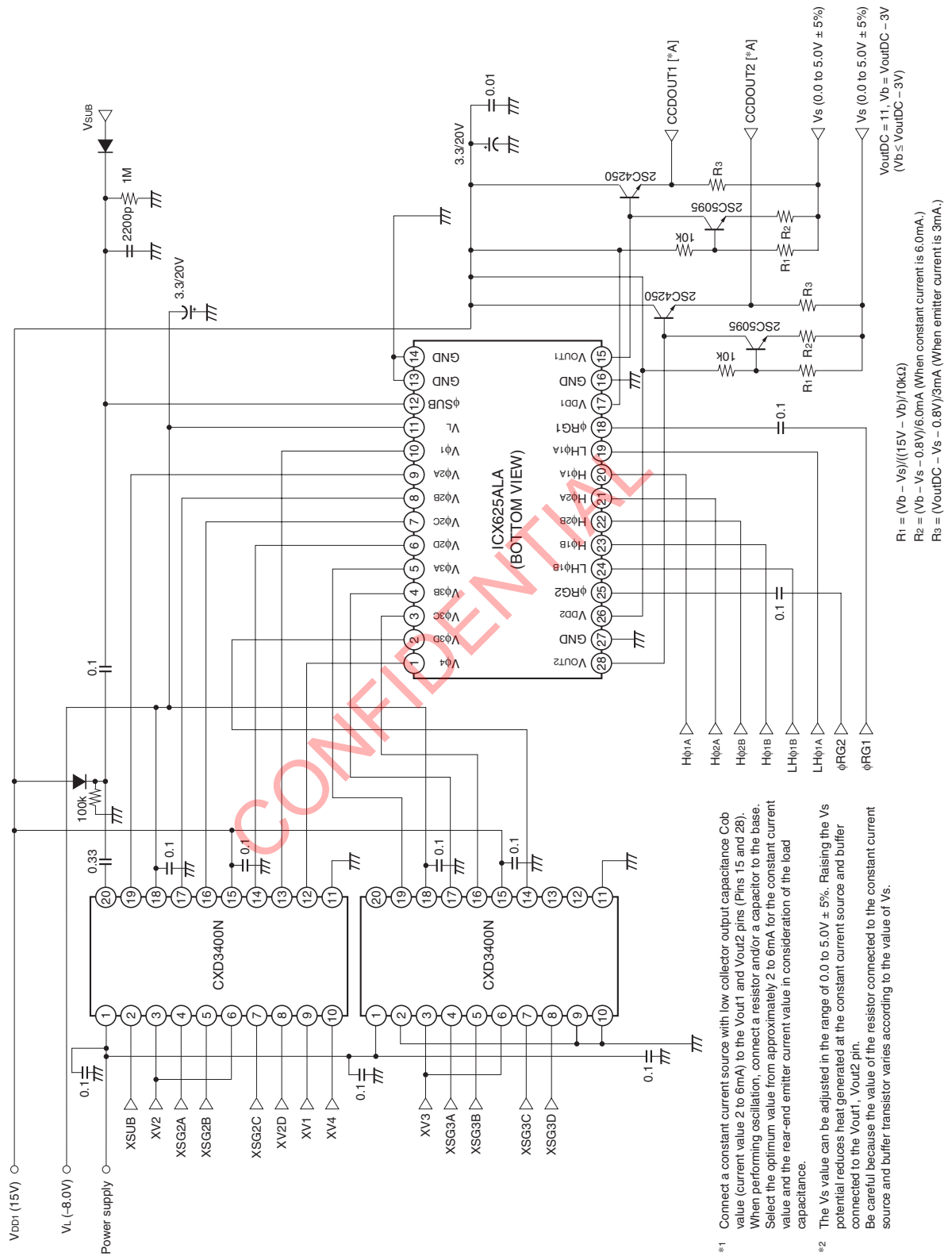
7. Lag

Adjust the signal output value generated by strobe light to 150mV. After setting the strobe light so that it strobes with the following timing, measure the residual signal (Vlag), and substitute the value into the following formula.

$$\text{Lag} = (\text{Vlag}/150) \times 100\ [\%]$$



Drive Circuit

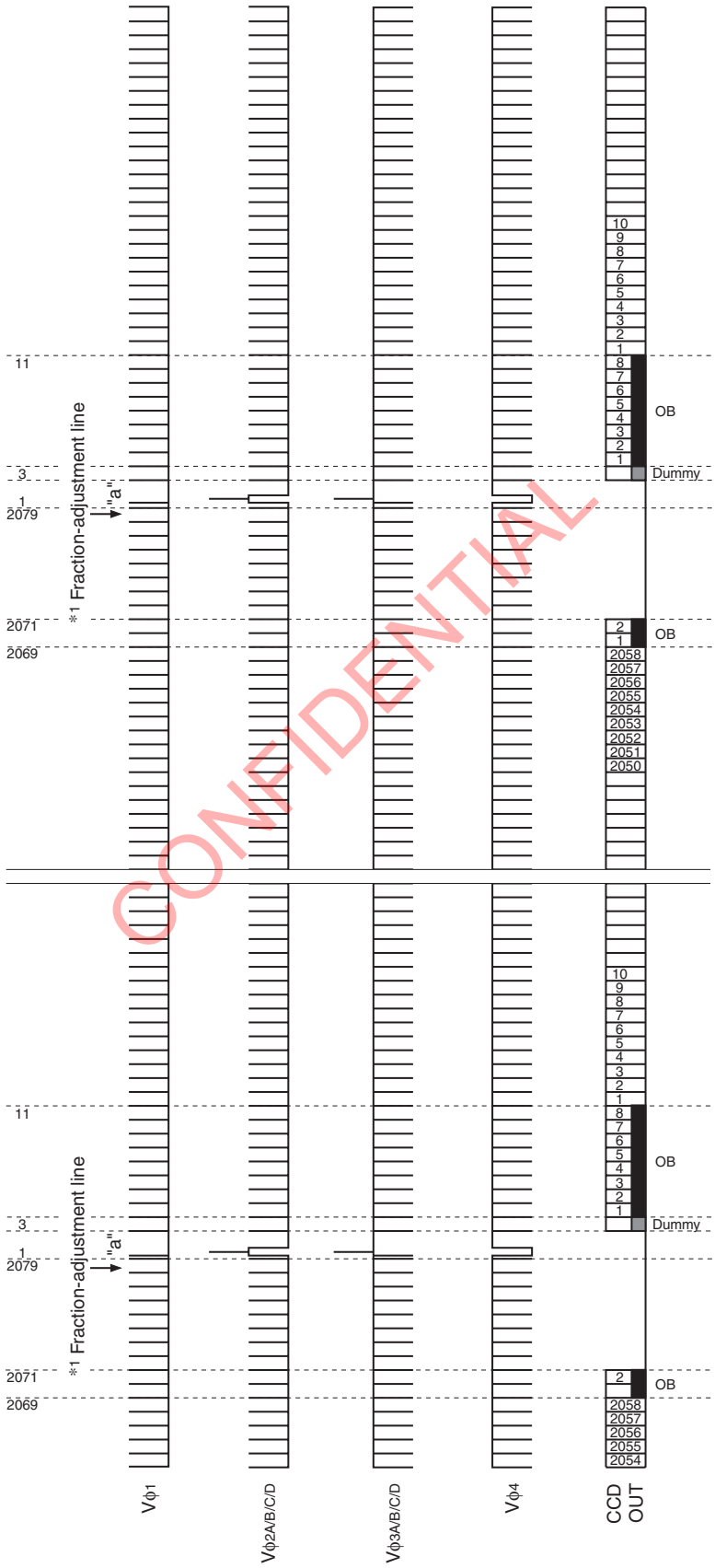


*1 Connect a constant current source with low collector output capacitance Cob value (current value 2 to 6mA) to the Vout1 and Vout2 pins (Pins 15 and 28). When performing oscillation, connect a resistor and/or a capacitor to the base. Select the optimum value from approximately 2 to 6mA for the constant current value and the rear-end emitter current value in consideration of the load capacitance.

*2 The Vs value can be adjusted in the range of 0.0 to 5.0V ± 5%. Raising the Vs potential reduces heat generated at the constant current source and buffer connected to the Vout1, Vout2 pin.
Be careful because the value of the resistor connected to the constant current source and buffer transistor varies according to the value of Vs.

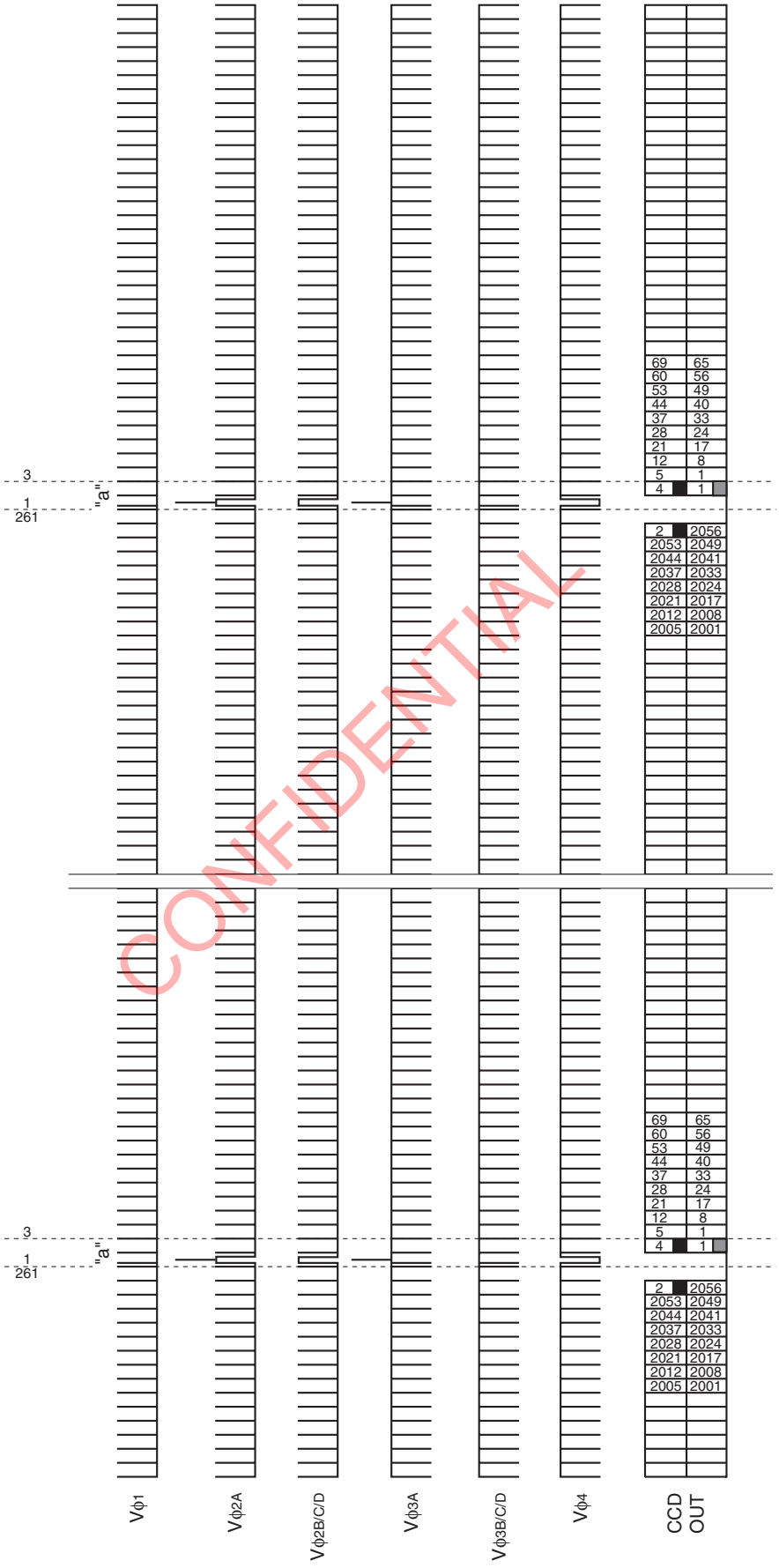
Drive Timing Chart

Vertical Sync, All-pixel Scan Mode, Horizontal Drive Frequency 60MHz, fh = 1924, fv = 2079

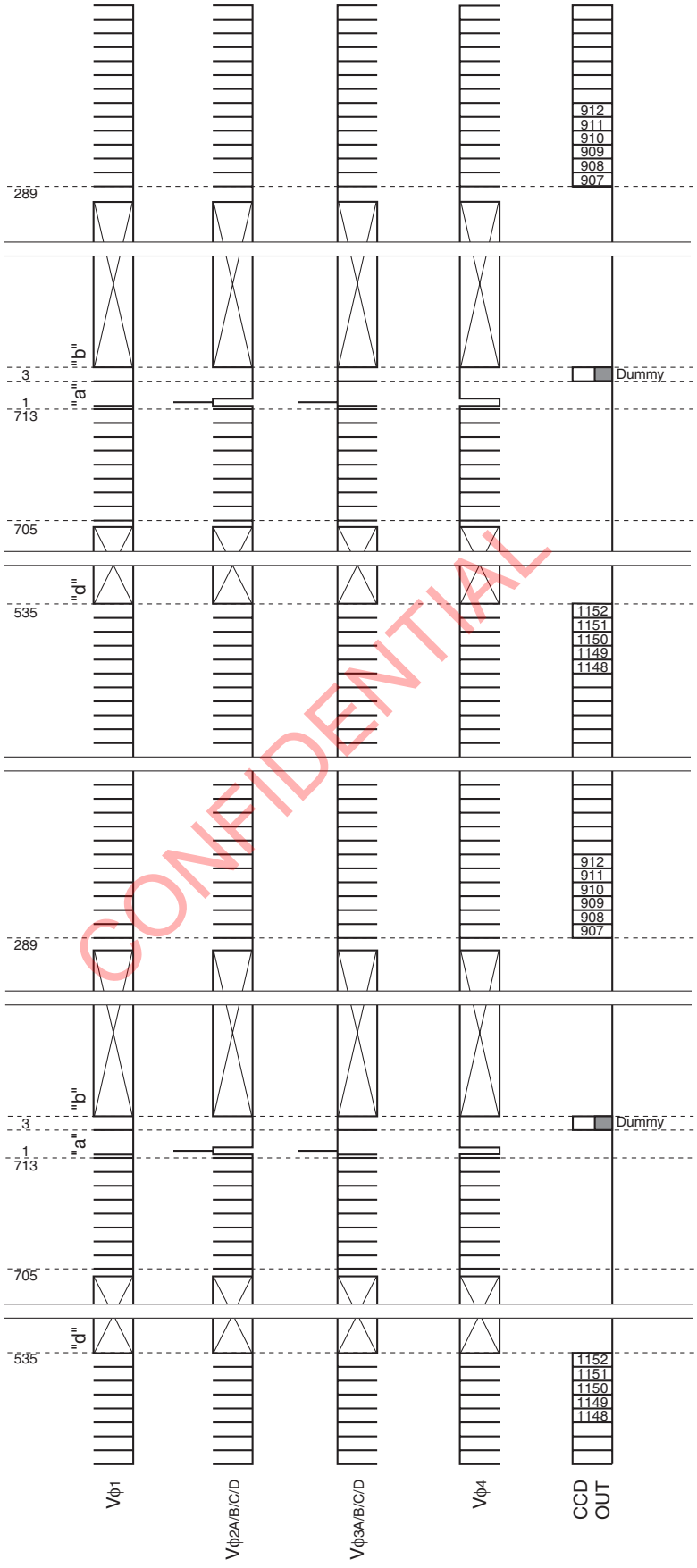


*1 When using at a frame rate of exactly 15.0fps, set the fraction-adjustment lines.
At the fraction-adjustment lines, fh = 1928bits, and thus the number of horizontal effective period clocks increases.

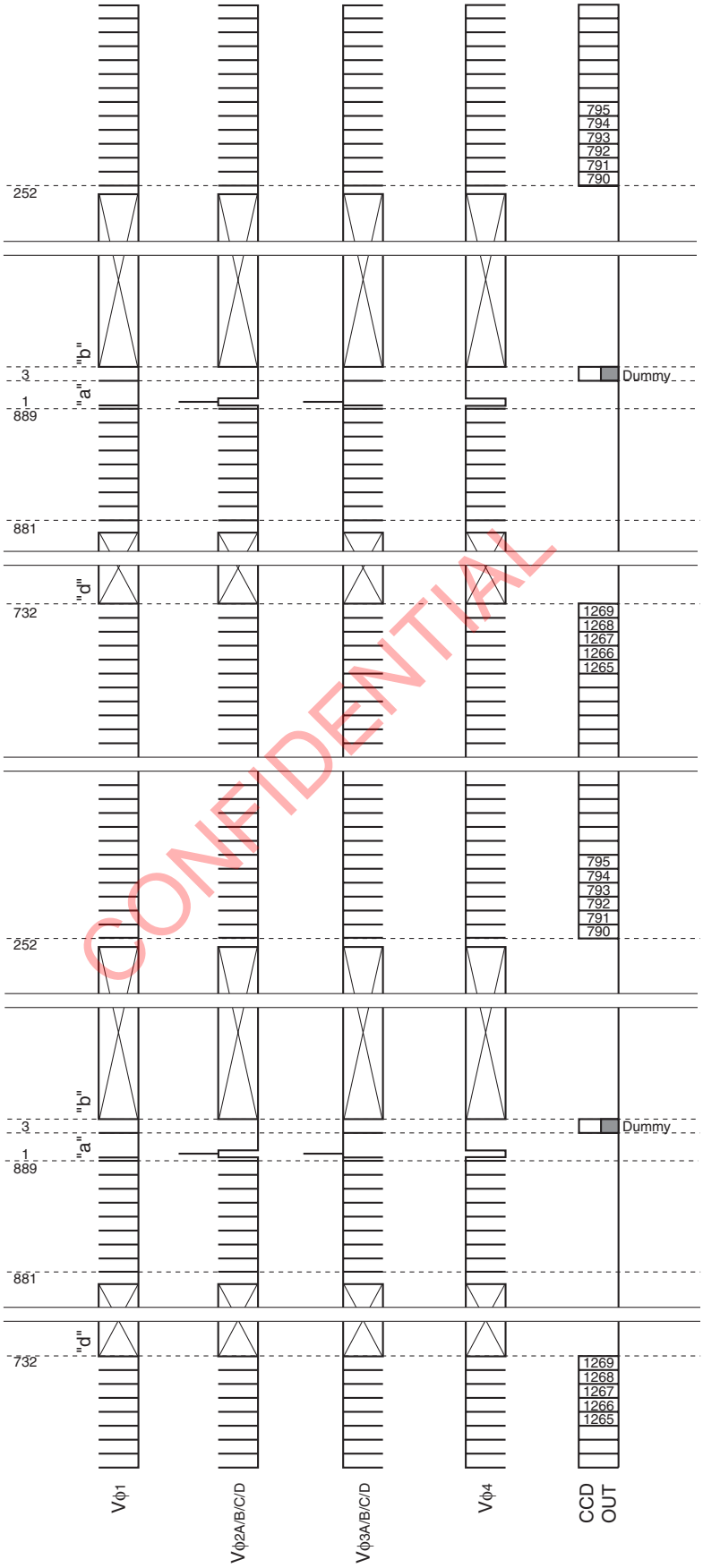
Vertical Sync, 4/16-line Readout Mode, Horizontal Drive Frequency 60MHz, fh = 6124, fv = 261



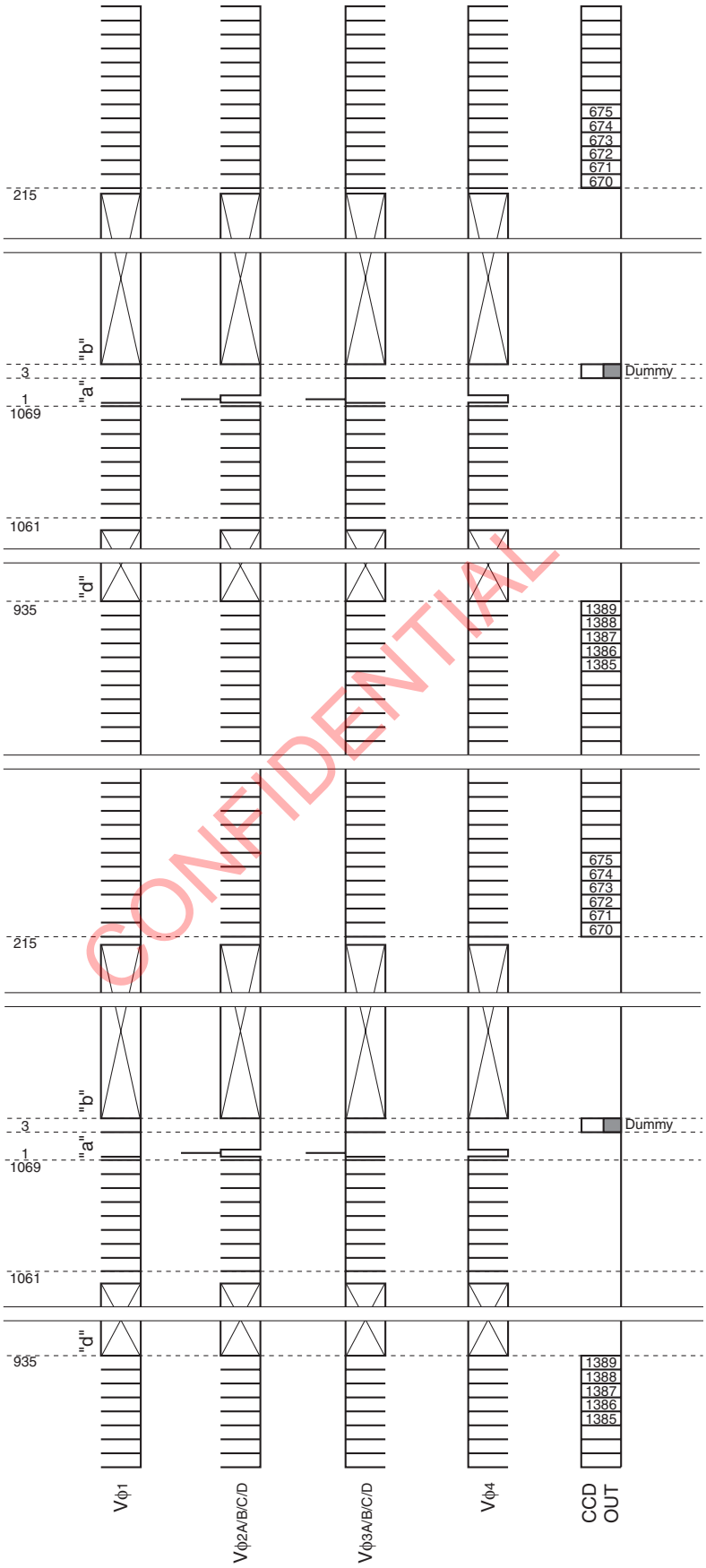
Vertical Sync, Center Scan Mode, when the Center 246 Lines are Cut Out,
Horizontal Drive Frequency 60MHz, fh = 1924, fv = 713



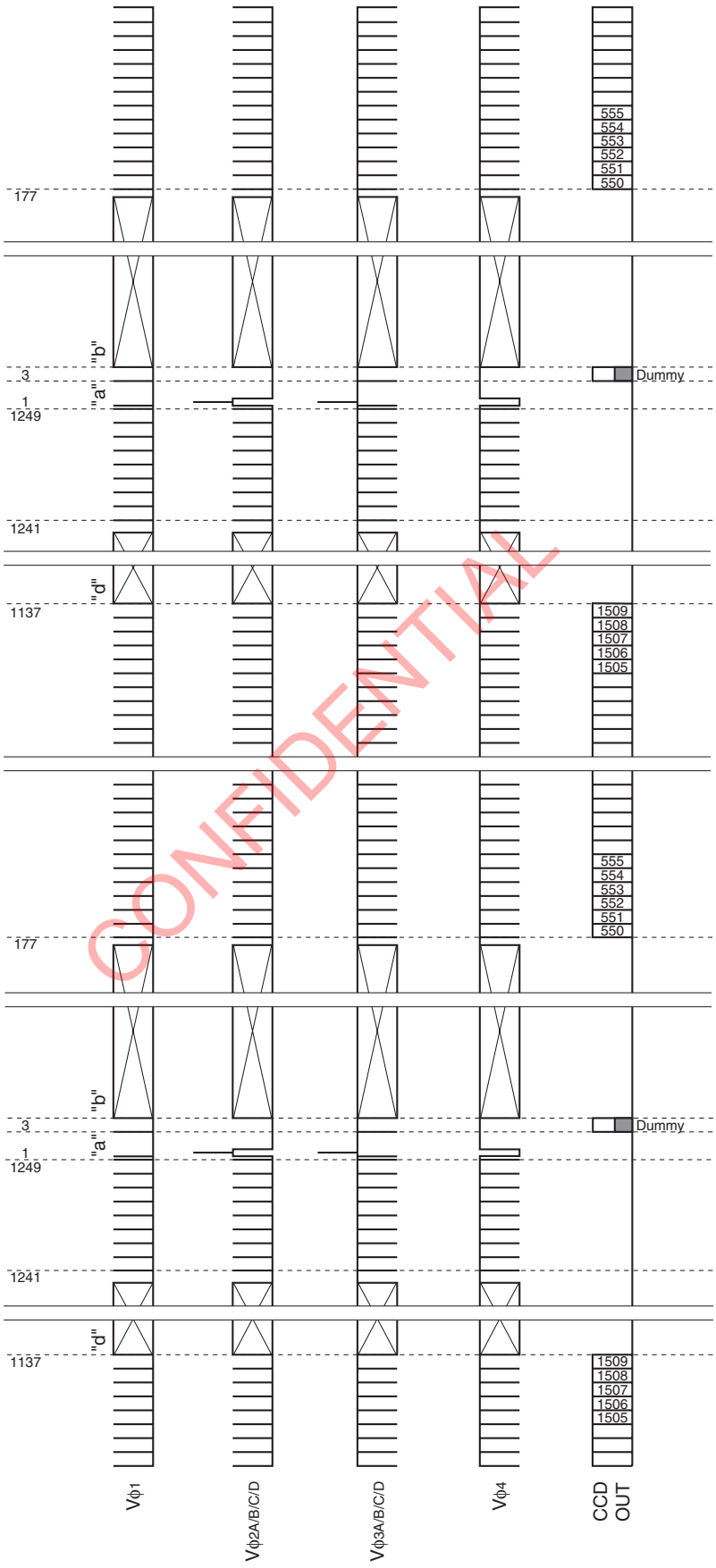
Vertical Sync, Center Scan Mode, when the Center 480 Lines are Cut Out,
Horizontal Drive Frequency 60MHz, fh = 1924, fv = 889



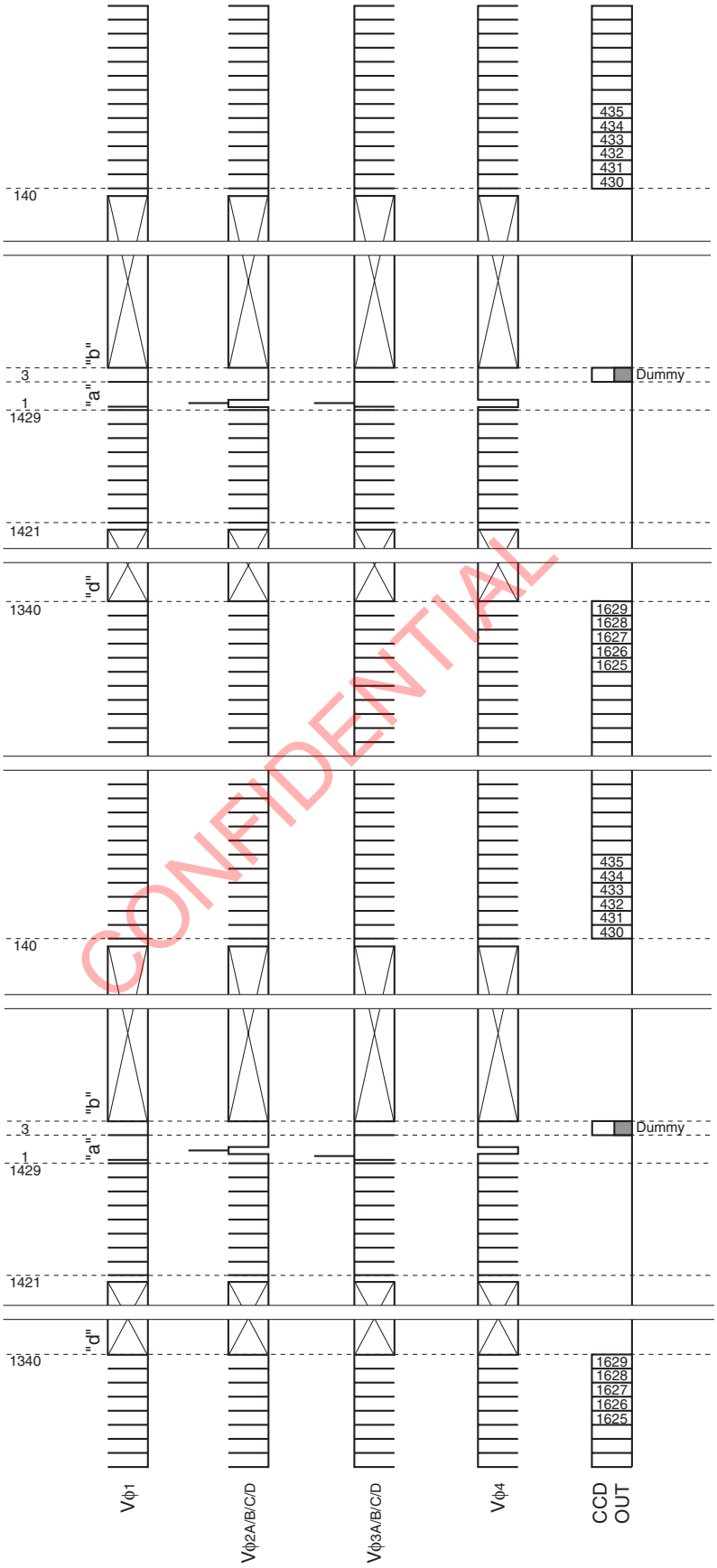
Vertical Sync, Center Scan Mode, when the Center 720 Lines are Cut Out,
Horizontal Drive Frequency 60MHz, fh = 1924, fv = 1069



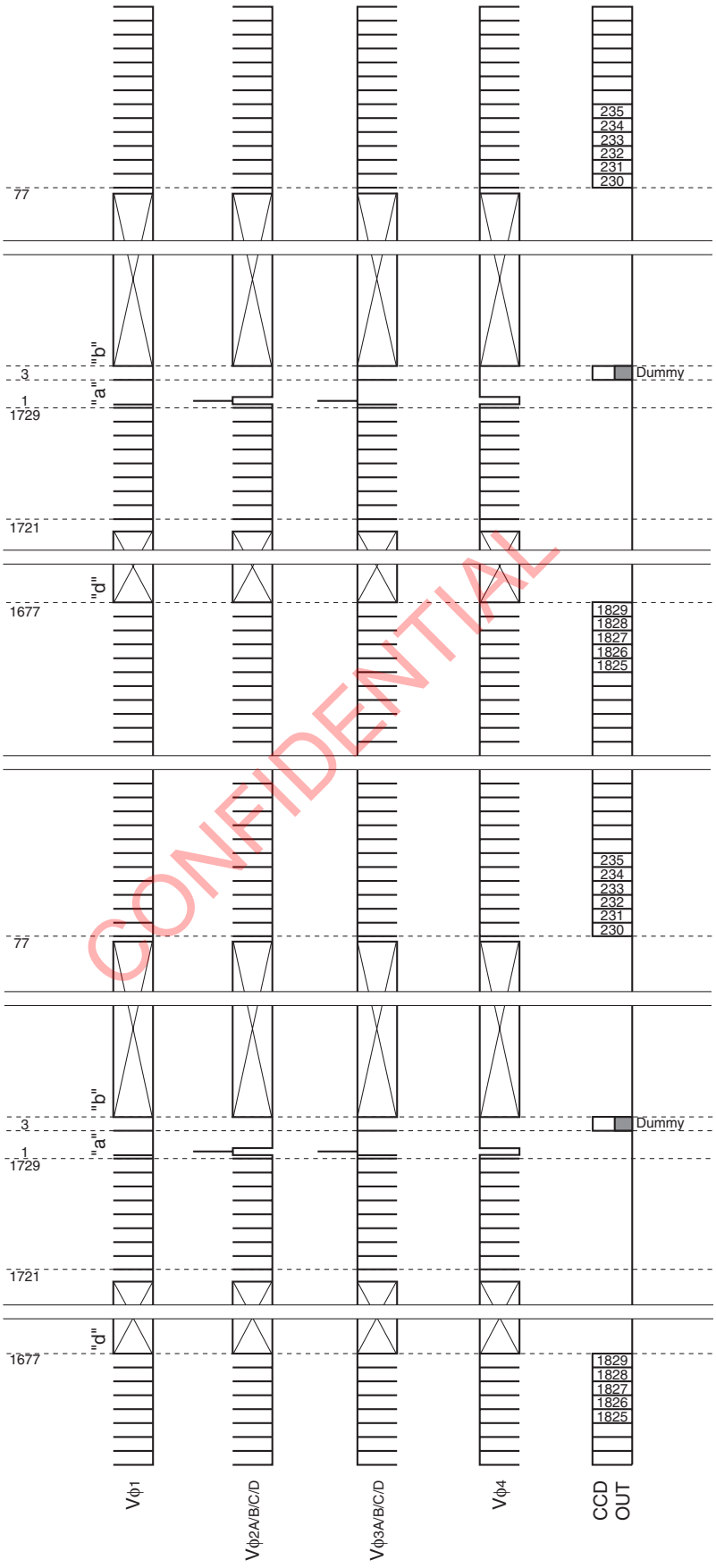
Vertical Sync, Center Scan Mode, when the Center 960 Lines are Cut Out,
Horizontal Drive Frequency 60MHz, fh = 1924, fv = 1249



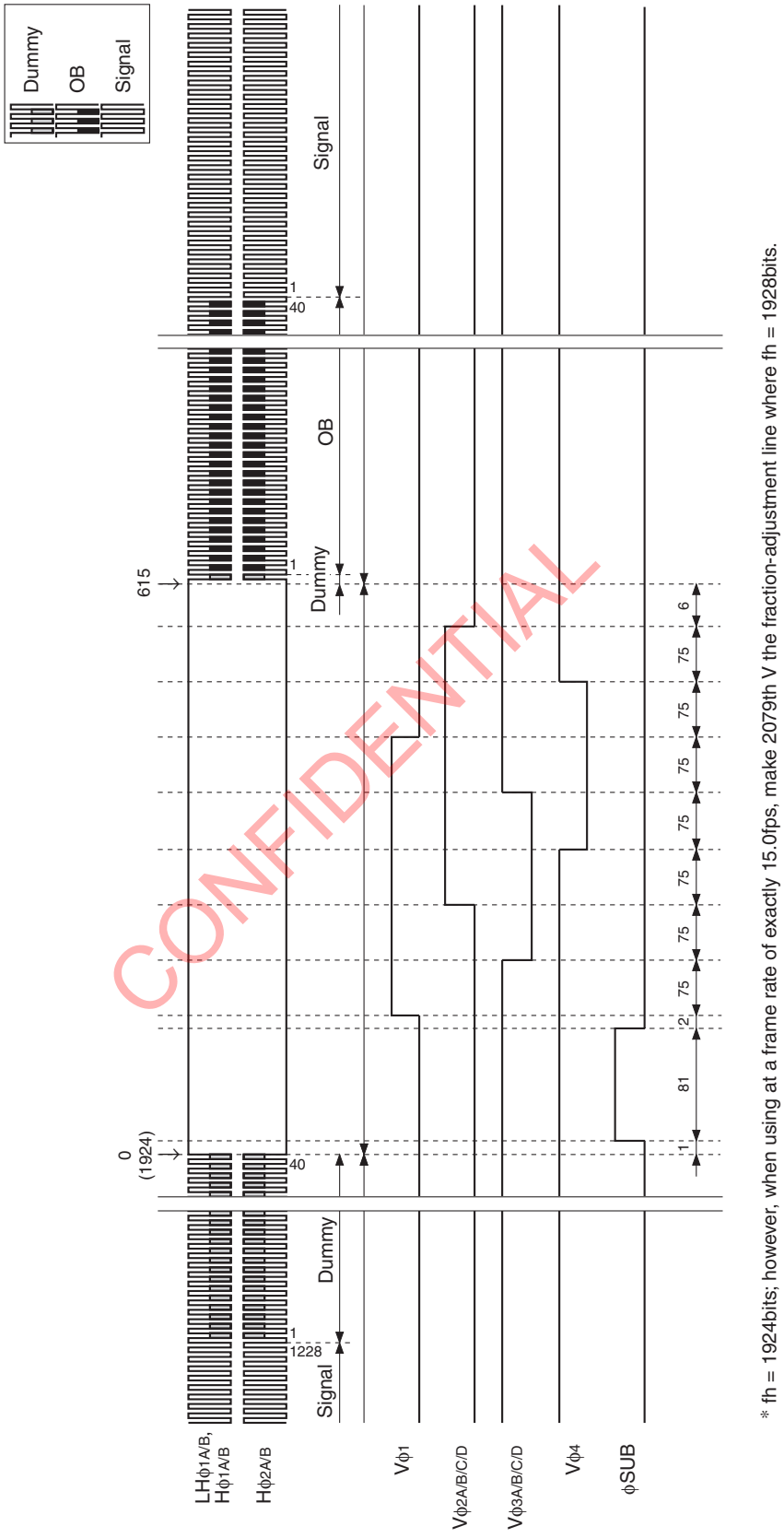
Vertical Sync, Center Scan Mode, when the Center 1200 Lines are Cut Out,
Horizontal Drive Frequency 60MHz, fh = 1924, fv = 1429



Vertical Sync, Center Scan Mode, when the Center 1600 Lines are Cut Out,
Horizontal Drive Frequency 60MHz, fh = 1924, fv = 1729

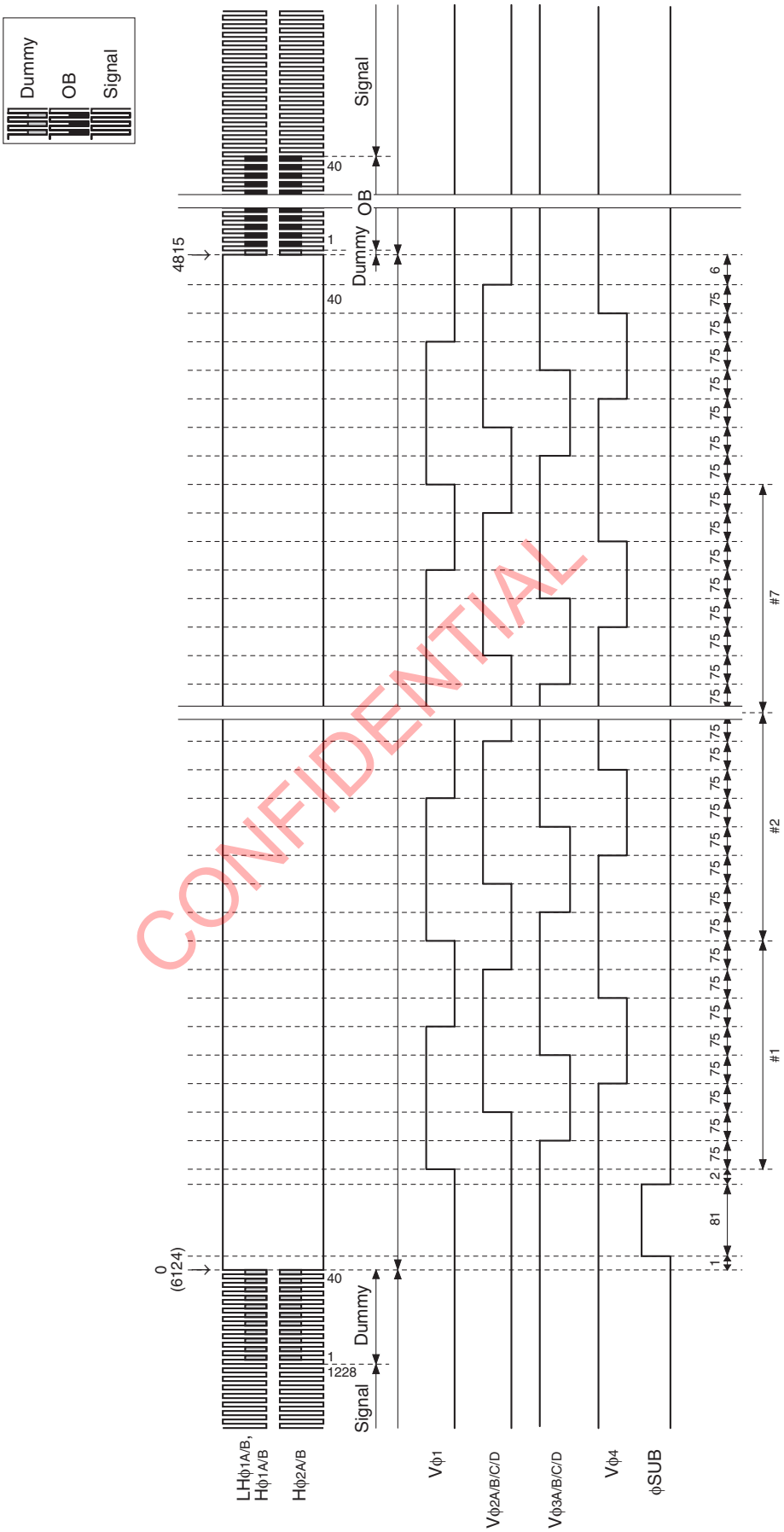


Horizontal Sync, All-pixel Scan Mode/Center Scan Mode, Horizontal Drive Frequency 60MHz, fh = 1924



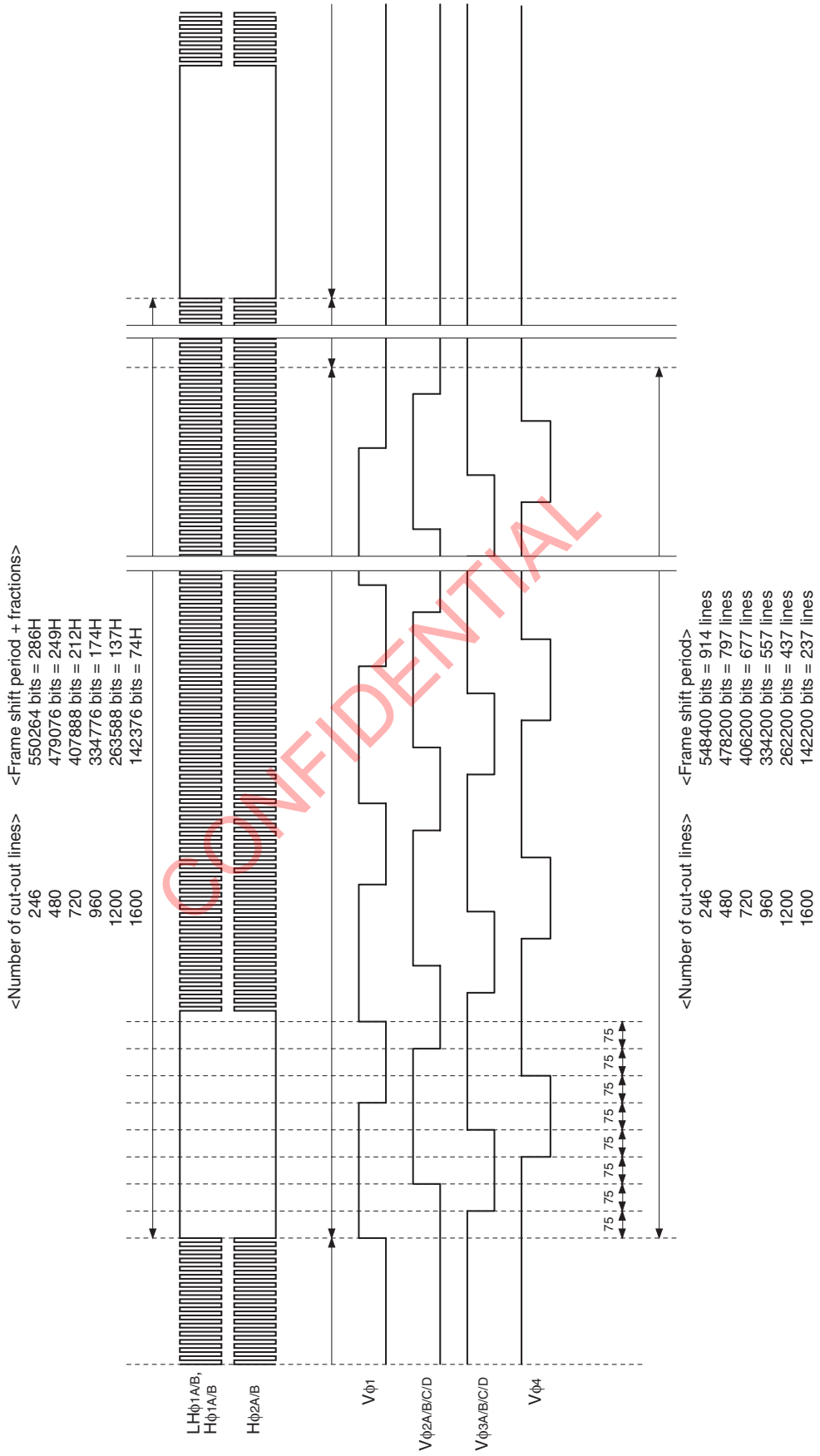
* fh = 1924bits; however, when using at a frame rate of exactly 15.0fps, make 2079th V the fraction-adjustment line where fh = 1928bits.

Horizontal Sync, 4/16-line Readout Mode, Horizontal Drive Frequency 60MHz, fh = 6124



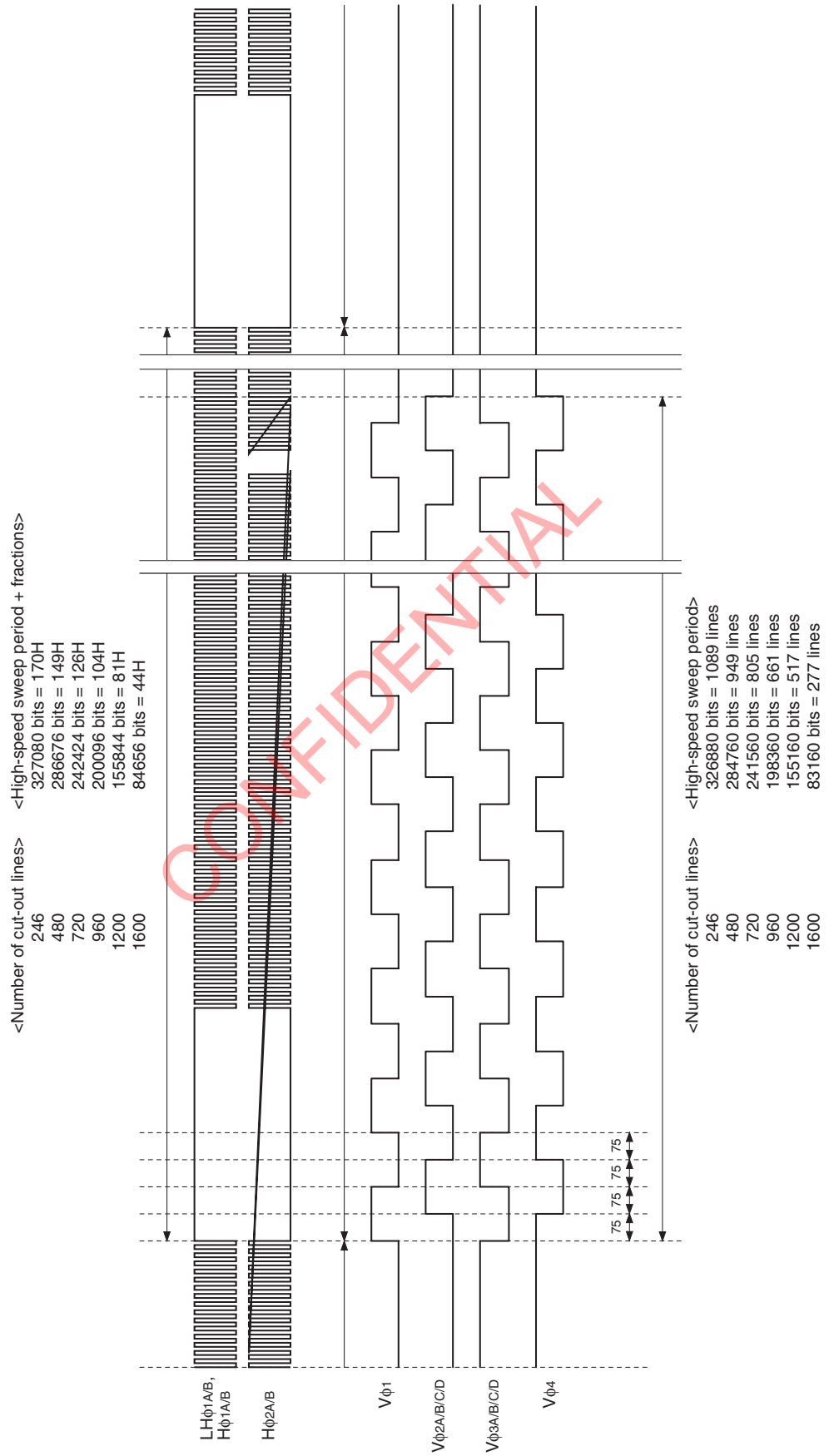
Horizontal Sync, Center Scan Mode, Horizontal Drive Frequency 60MHz, fh = 1924

(Vertical Sync “b” Enlarged)



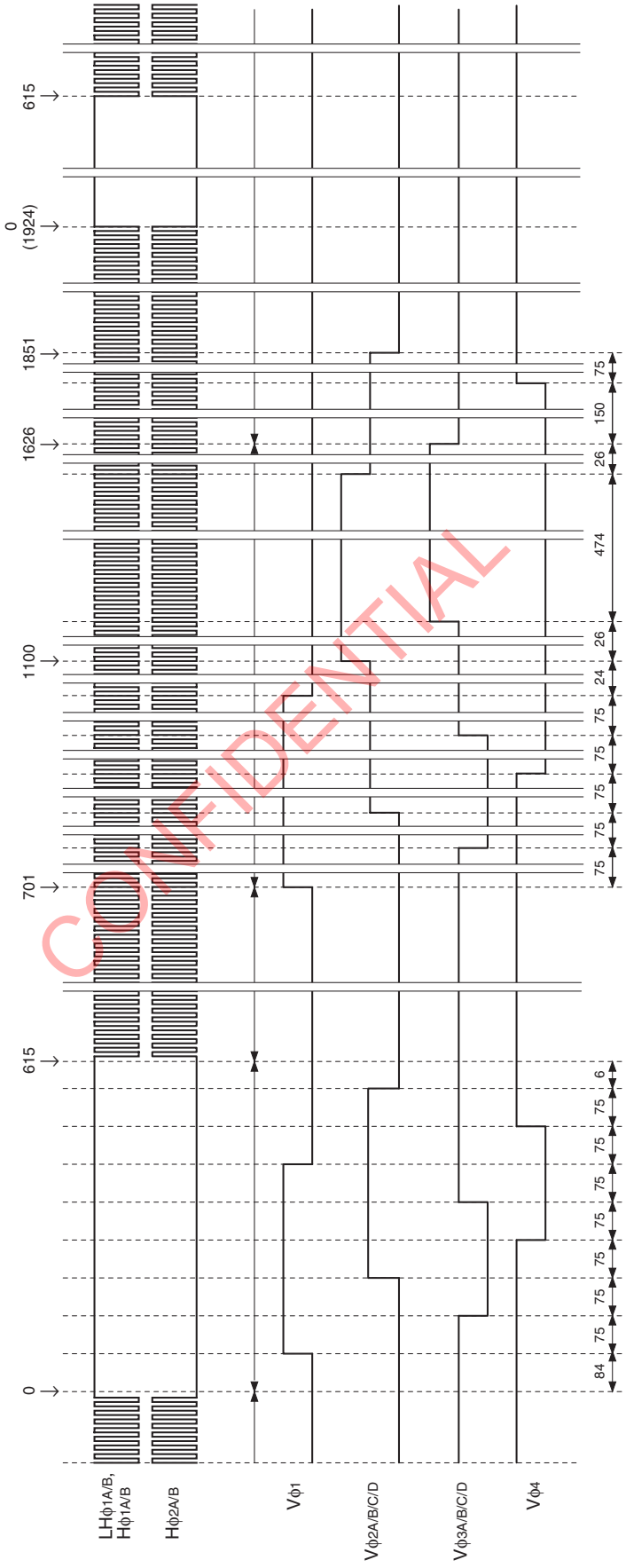
Horizontal Sync, Center Scan Mode, Horizontal Drive Frequency 60MHz, fh = 1924

(Vertical Sync "d" Enlarged)



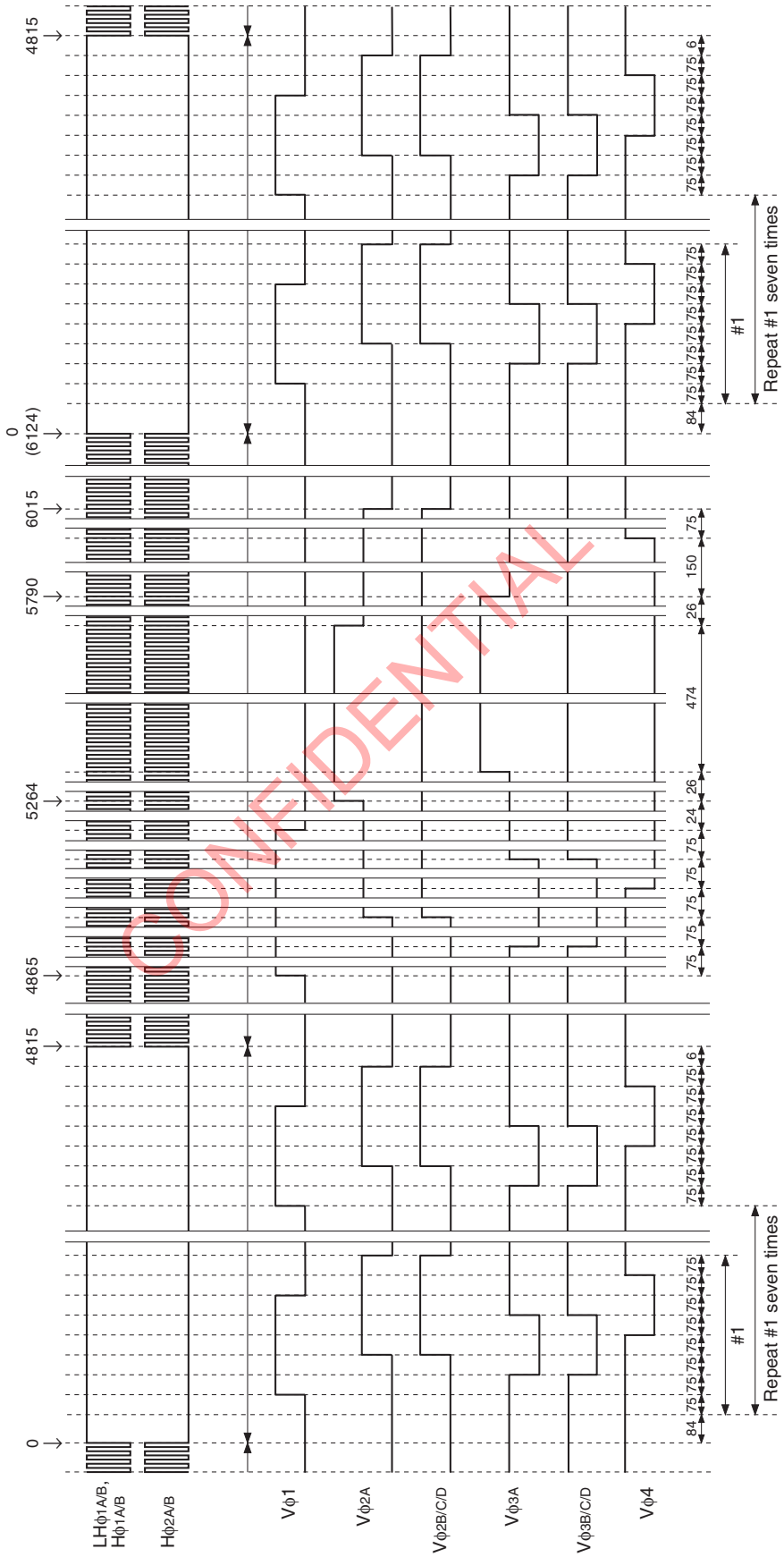
Vertical Sync, All-pixel Scan Mode/Center Scan Mode, Horizontal Drive Frequency 60MHz, fh = 1924

(Vertical Sync "a" Enlarged)



Vertical Sync, 4/16-line Readout Mode, Horizontal Drive Frequency 60MHz, fh = 6124

(Vertical Sync "a" Enlarged)



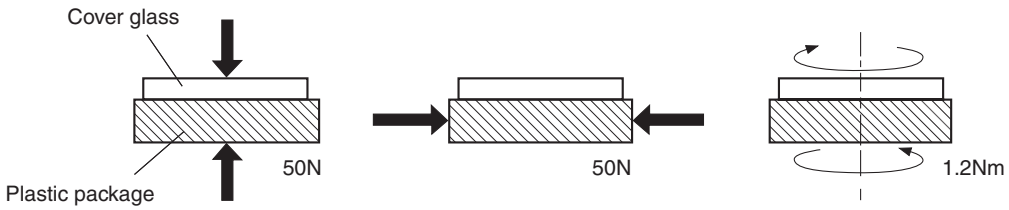
Notes On Handling

1. Static charge prevention
   Image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.
   (1) Either handle bare handed or use non-chargeable gloves, clothes or material. Also use conductive shoes.
   (2) Use a wrist strap when handling directly.
   (3) Install grounded conductive mats on the floor and working table to prevent the generation of static electricity.
   (4) Ionized air is recommended for discharge when handling image sensors.
   (5) For the shipment of mounted boards, use boxes treated for the prevention of static charges.

2. Soldering
   (1) Make sure the temperature of the upper surface of the seal glass resin adhesive portion of the package does not exceed 80℃.
   (2) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a 30W soldering iron with a ground wire and solder each pin in 2 seconds or less. For repairs and remount, cool sufficiently.
   (3) To dismount an image sensor, do not use solder suction equipment. When using an electric desoldering tool, use a thermal controller of the zero-cross On/Off type and connect it to ground.

3. Protection from dust and dirt
   Image sensors are packed and delivered with care taken to protect the element glass surfaces from harmful dust and dirt. Clean glass surfaces with the following operations as required before use.
   (1) Perform all lens assembly and other work in a clean room (class 1000 or less).
   (2) Do not touch the glass surface with hand and make any object contact with it. If dust or other is stuck to a glass surface, blow it off with an air blower. (For dust stuck through static electricity, ionized air is recommended.)
   (3) Clean with a cotton bud and ethyl alcohol if grease stained. Be careful not to scratch the glass.
   (4) Keep in a dedicated case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
   (5) When a protective tape is applied before shipping, remove the tape applied for electrostatic protection just before use. Do not reuse the tape.

4. Installing (attaching)
   (1) Remain within the following limits when applying a static load to the package. Do not apply any load more than 0.7mm inside the outer perimeter of the glass portion, and do not apply any load or impact to limited portions. (This may cause cracks in the package.)



Compressive strength **Torsional torque**

   (2) If a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the bottom of the package. Therefore, for installation, use either an elastic load, such as a spring plate, or an adhesive.
   (3) The adhesive may cause the marking on the rear surface to disappear, especially in case the regulated voltage value is indicated on the rear surface. Therefore, the adhesive should not be applied to this area, and indicated values should be transferred to the other locations as a precaution.

(4) The notch of the package is used for directional index, and that can not be used for reference of fixing. In addition, the cover glass and seal resin may overlap with the notch of the package.

(5) If the lead bend repeatedly and the metal, etc., clash or rub against the package, dust may be generated by the fragments of resin.

(6) Acrylate anaerobic adhesives are generally used to attach image sensors. In addition, cyanoacrylate instantaneous adhesives are sometimes used jointly with acrylate anaerobic adhesives to hold the image sensor in place until the adhesive completely hardens. (reference)

5. Others

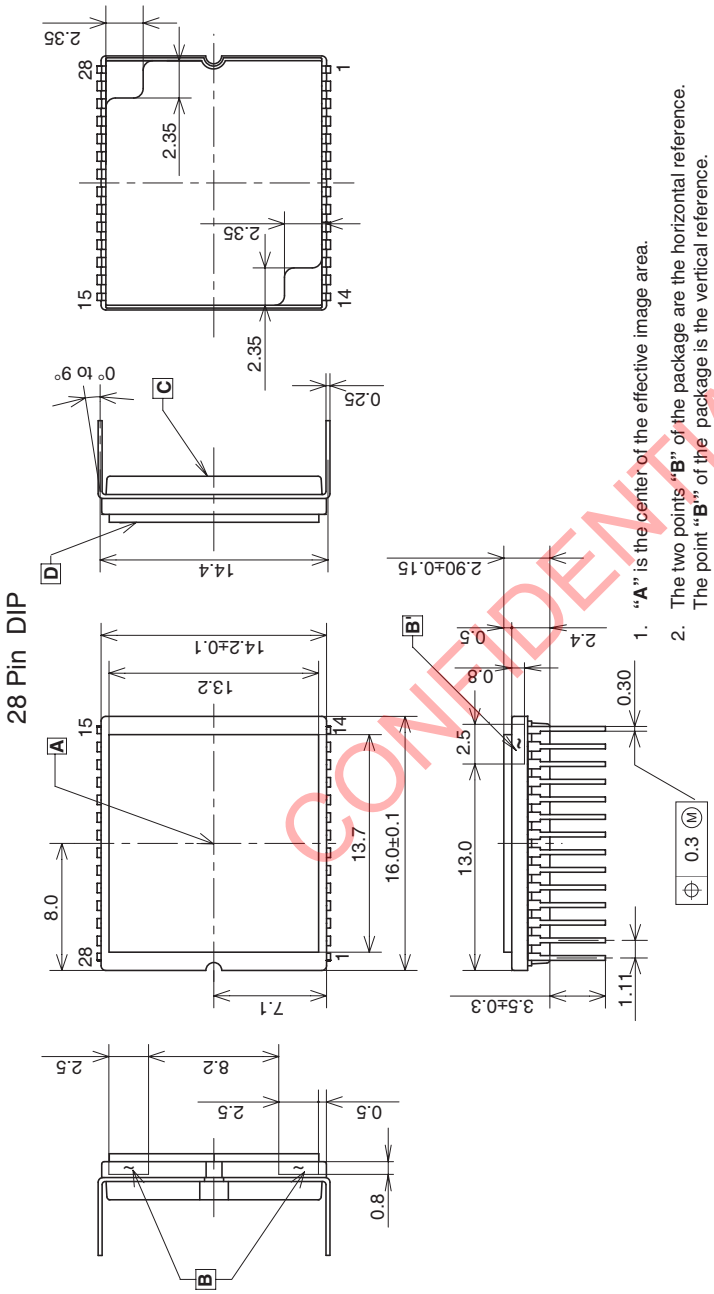
(1) Do not expose to strong light (sun rays) for long periods, as color filters will be discolored. When high luminance objects are imaged with the exposure level controlled by the electronic iris, the luminance of the image-plane may become excessive and discoloration of the color filters may be accelerated. In such a case, arrangements such as using an automatic iris with the imaging lens or automatically closing the shutter during power-off are advisable. For continuous use under harsh conditions exceeding the normal conditions of use, consult your Sony representative.

(2) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or use in such conditions.

(3) Brown stains may be seen on the bottom or side of the package. But this does not affect the characteristics.

Package Outline

(Unit: mm)



1. **"A"** is the center of the effective image area.
2. The two points **"B"** of the package are the horizontal reference.
   The point **"B"** of the package is the vertical reference.
3. The bottom **"C"** of the package and the top of the cover glass **"D"** are the height reference.
4. The center of the effective image area relative to **"B"** and **"B'"** is (H, V) = (8.0, 7.1)±0.075mm.
5. The rotation angle of the effective image area relative to H and V is±1°.
6. The height from the bottom **"C"** to the effective image area is 1.41±0.10mm.
   The height from the top of the cover glass **"D"** to the effective image area is 1.49±0.15mm.
7. The tilt of the effective image area relative to the bottom **"C"** is less than 50µm.
   The tilt of the effective image area relative to the top **"D"** of the cover glass is less than 50µm.
8. The thickness of the cover glass is 0.5mm, and the refractive index is 1.5.
9. The notch of the package is used only for directional index, that must not be used for reference of fixing.

PACKAGE STRUCTURE

PACKAGE MATERIAL	Plastic
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	1.20g
DRAWING NUMBER	AS-A13-01(E)