DRAGSTER LINESCAN SENSOR

short spec sheet

Part name	:	DRAGSTER LINESCAN SENSOR
Covered versions	:	DR-2k-7LCC; DR-2k-7-invar; DR-4k-7; DR-8k-7 DR-4k-3.5LCC; DR-4k-3.5-invar; DR-8k-3.5; DR-16k-3.5 DR-2x2k-7LCC; DR-2x2k-7-invar; DR-2x4k-7, DR-2x8k-7 DR-2x2k-7LCC-RGB; DR-2x2k-7-invar-RGB; DR-2x4k-7-RGB, DR-2x8k-7-RGB
Revision	:	3.10
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1 Contents

2 Introduction

This document is for evaluation purpose only!
do request the full data sheet prior to design in.

DRAGSTER is a platform of a digital line-scan sensors. The Sensor family is organized such that line-scan sensor with basic elements of 1x 2k pixels respectively 2x 2k pixels with 7um pitch or 1x 4k pixels with 3.5um pitch can be easily realized. E.g. sensors with pixel numbers of:

1x 2k; 1x 4k; 1x 6k; 1x 8k; 1x 12k; 1x 16k;
2x 2k; 2x 4k, 2x 6k; 2x 8k; 2x 12k;

are possible. The chip versions with dual line readout are optionally available with Bayer pattern RGB filters placed on the sensors.

For all variations the basic readout and control electronics are identical. Further different variations of pixel aspect ratios can be implemented. Please contact AWAIBA if you should require customized resolution sensors.

The current specification covers the following device variations:

Part Number	**Number of pixels**	**Pixel size**	**Package Type**
DR-2k-7LCC	1x2048	7um x 7um	LCC
DR-2k-7-invar	1x2048	7um x 7um	Invar module
DR-4k-7	1x4096	7um x 7um	Invar module
DR-8k-7	1x8192	7um x 7um	Invar module
DR-4k-3.5LCC	1x4096	3.5um x 3.5um	LCC
DR-4k-3.5-invar	1x4096	3.5um x 3.5um	Invar module
DR-8k-3.5	1x8192	3.5um x 3.5um	Invar module
DR-16k-3.5	1x16384	3.5um x 3.5um	Invar module
DR-2x2k-7LCC	2x2048	7um x 7um	LCC
DR-2x2k-7-invar	2x2048	7um x 7um	Invar module
DR-2x4k-7	2x4096	7um x 7um	Invar module
DR-2x8k-7**	2x8192	7um x 7um	Invar module
DR-2x2k-7-LCC-RGB	2x2048	7um x 7um	LCC
DR-2x2k-7-invar-RGB	2x2048	7um x 7um	Invar module
DR-2x4k-7-RGB	2x4096	7um x 7um	Invar module
DR-2x8k-7-RGB	2x8192	7um x 7um	Invar module

** sales restrictions may apply to Japan

The sensor features a low noise pixel with true CDS and global shutter for interleaved readout and integration operation. Each pixel has an on pixel ADC and 13bit readout register. AD conversion is made to 12.2 bits and for output clamped to 12bit to guarantee full 4096 DN signal swing. The ADC gain can be programmed in a range of -6dB till + 20 dB by means of an 8bit DAC controlled over the serial configuration interface.

The readout is made by 2 12bit wide digital taps organized in odd / even order for each 2k segment. (full 13 bit readout is possible for special purposes) For each line segment, all 2k pixels have to be read out.

For sensor versions with 3.5um pixel pitch, two 2k segment readout circuits are placed on each side of the pixel line, to lead to a basic segment of 4k pixels, even pixels read out over the bottom readout, odd pixels read out over the top readout.

Start of integration, end of integration and optional start of readout are started upon individual external trigger events. To enhance dynamic range multiple non destructive readouts are possible.

3 Electrical Description

The sensor will comply to the specifications listed in this section within the operating ranges listed in the respective section.

An applied signal must not have a deviation from the ideal signal, at the pin of the circuit, such that the circuit or the parameter under test are affected significantly.

Proper decoupling of the circuit according to section Error: Reference source not found is required. The following section defines the limits of functional operation and parametric characteristics of the circuit, and reliability. Note that functionality of the circuit outside the operating range as specified in this section is not guaranteed.

3.1 Absolute Maximum Ratings

Stresses above those listed in this clause may cause immediate and permanent device failure. Operation outside the operating conditions for extended periods may affect device reliability. It is not implied that more than one of these conditions can be violated simultaneously.

Total cumulative dwell time above the maximum operating rating for temperature must be less than 100 hours.

Symbol	Description	Min	Max	Unit
VDD	Power supply voltage (digital)	-0.3	3.6	V
VIO	Voltage on any IO	-0.3	VDDIO +0.3 or 3.6	V
IIO	DC forward BIAS current, input or output		-24 (source) +24 (sink)	mA
Tj	Junction temperature	-55	125	°C

3.2 Electrical overstress immunity

Electrostatic discharges on component level:
The device withstands 1k Volts Human Body Model ESD pulses when tested according to MIL STD 883 method 3015.7 .

3.3 Latch-up immunity

Static latch-up protection level is 10mA at 25°C when tested according to EIA/JESD78.

3.4 Power on Sequence

The correct fully sequential power on sequence for all devices in INVAR headboard package is:

1) VDDESD
2) VDDA
3) VDD_BULK
4) VDDD
5) VDDIO
6) ramp up signals on any inputs
7) release N_RESET_XX

A simplified power on sequence is:

1) VDDESD
2) VDD_BULK; VDDA; VDDD; VDDIO
3) ramp up signals on any inputs
4) release N_RESET_XX

For the LCC package versions, it is important that VDD ramps prior to any digital input signal.

In any condition the two following situations are to be avoided:

Fault A: Any VDDx is supplied before VDDESD or to a higher value than VDDESD.
Fault B: Digital inputs are supplied prior to supply of VDDESD.

3.5 Operating Conditions

Functional operation is guaranteed under these conditions.

Symbol	Description	min	typical	max	unit
VDDD	Power supply voltage (digital)	3.2	3.3	3.4	V
VDDA	Power supply voltage (analogue)	3.2	3.3	3.4	V
VDDESD	Power supply voltage ESD	3.2	3.3	3.4	V
VDDIO	Power supply voltage IO	2.4*	3.3	3.4	V
GND	Ground supply		0		V
Fclk	Input Clock Frequency Silicon Revision 2C	1**		46***	MHz
Fclk	Input Clock Frequency Silicon Revision 2E	1**		85	MHz
Duty_clk	Input Clock Duty cycle	45	50	55	%
Jitter_clk	Input Clock Jitter			100	ps
Cload	Load capacitance on digital I/O's			10	pF
Tj	Junction temperature	0	27	+80	°C
VnrmsVDDD	RMS Noise on VDD digital			20	mV
VnppVDDD	Peak to Peak Noise on VDD digital			100	mV
VnrmsVDDA	RMS Noise on VDD analogue			5	mv
VnppVDDA	Peak to Peak Noise on VDD analogue			20	mv
VnrmsVDD/IO	RMS Noise on VDD I/O			20	mv
VnppVDD/IO	Peak to Peak Noise on VDD I/O			100	mv
Vil	Low level input voltage	-0.3	0	0.4	V
Vih	High level input voltage	0.8*VDD/IO	VDD/IO	VDD/IO +0.3	V

* VDDIO < 3.0V is not recommended for pixel_clock speeds above 40MHz and may not meet the slew rate specifications in all cases.
** Fclk can be lower then 1MHz however the ADC conversion accuracy might be reduced.
*** the ADC can be clocked with up to 100MHz for faster conversion when using clock reduction for readout.

3.6 Electrical characteristics

Current consumptions are for one segment of 2k pixels. multiples apply for higher resolution sensors.

Symbol	Description	Min	Max	Unit
Vol	Low level output voltage *		0.5	V
Voh	High level output voltage *	VDD/IO-0.6		V
Iil	Low level input leakage (Vi=0)		+-1	uA
Iih	High level input leakage (Vi=VDD/IO)		+-1	uA
tslew, rising	Output slew rate of rising edge*		5	ns
tslew, falling	Output slew rate of falling edge*		5	ns
Ptot**	Power Consumption per 2k segment		400	mW
I (VDDA)	Current to analog devices per 2k segment		50	mA
I (VDDD)	Current to Digital devices per 2k segment		30	mA
I (VDDIO)	Current for I/O per 2k segment		40	mA
I (VDD_bulk)	Current over bulk contacts, nominal no DC current, should be designed to support equal current to VDDD			
I (VDDESD)	Current of ESD protection, nominal no DC current, should be designed to support equal current to VDDD			

* The output swing on signal pixel_clock (if enabled) may be smaller at pixel clock rates above 60MHz

Resulting maximum current consumption for the different chip variations:

Part Number	**I(VDDA) / mA**	**I(VDDD) / mA**	**I(VDDIO) / mA** *	**Ptot /mW** ** (total power consumption)
DR-4k-7	100	60	80	800
DR-8k-7	200	120	160	1600
DR-8k-3.5	200	120	160	1600
DR-16k-3.5	500	240	320	3500
DR-2x4k-7	200	120	160	1600
DR-2x8k-7	500	240	320	3500

Part Number	**I(VDD) / mA**	**Ptot /mW** ** (total power consumption)
DR-2k-7	120	400
DR-4k-3.5	240	800
DR-2x2k-7	240	800

* @ 10pF
** At VDDDIO = 3.3V 46MHz Cload dig 10pF 20% I/O activity

3.7 Optical characteristics DR-2k-7LCC; DR-4k-7; DR-8k-7

Parameter	Min	Typ/ Target	Max	unit
Pixel size		7 x 7		um
Pixel pitch in x direction		7		um
Number of dark pixels in most left segment		32		pixels
Fill Factor		100		%
Quantum efficiency at 630nm	50	60	70	%
Full Well capacity(4)	30	46	65	ke-
Total System Gain K		0.076		DN/e-
DSNU rms (1;5)		4	10	DN/12bit
Responsivity (1)		77		DN/nJ/cm2 (@12bit)
Responsvity analogue gain 4x (6)		310		DN/nJ/cm2 (@12bit)
PRNU rms (1;5)		0.7%	3%	% (full scale)
PRNU pp (1; 5)		4%	8%	% (full scale)
ADC Programmable gain	-6		20	dB
ADC gain resolution		8		bit
Blooming overload tolerance	100x	infinite		
Lag		0	0.01	%
Crosstalk (optical & electrical)		2	5	%
Exposure time range	2		infinite	us
Temporal noise Dark rms (2)*		1.5	4	DN/12bit
Dark noise electrons rms (2)*		22		e-
NEE (noise equivalent energy) unity gain (1)		0.02		nJ/cm2
Temporal noise Dark rms gain 4x (6)*		2.9	5	DN/12bit
Dark noise electrons rms gain 4x (6)*		7		e-
NEE (noise equivalent energy) analogue gain x4 (6)*		0.01		nJ/cm2
Non Linearity (3)		2	5	%
Dark current @27C		3	50	e-/ms
Maximum Line Rate			80	kScan/s
ADC Resolution		12 (13)***		bit
Number of output taps		2per 2k segment		
Configuration Interface		Serial 4 line (1 interface / 2k segment)		
Integration control		Asynchronous, with 6 digital signals		
Trigger delay			1	us
Integration & Readout		Interleaved		

(1) Tint=10us, Unity gain (CDS_gain = 0 -> x1; Inverse ADC gain = 0x20h)
(2) T=27ºC , Tint=20us, Unity gain (CDS_gain = 0; -> x1 Inverse ADC gain = 0x20h)
(3) Measured in % deviation from full scale signal for the signal range of 5% - 95% (according to EMVA1288 proposal for linearity measurement)

(4) At unity gain (CDS_gain = 0 -> x1; Inverse ADC gain = 0x20h; end counter 128 (4096 ADC levels))

(5) Ramp offset and ramp gain must be adjusted for all segments to match with each other.

(6) T=27ºC , Tint=20us, Unity gain (CDS_gain = 1; -> x4 Inverse ADC gain = 0x20h)

* {info only: temporal noise can further be reduced by subtracting from each line the average value of the dark reference pixels, which will reduce temporal noise components coupled over the supply at frequencies below the line rate. :end info}

*** internal ADC resolution is 13bit.

3.8 Optical characteristics DR-2x2k-7LCC; DR-2x4k-7; DR-2x8k-7

Parameter	Min	Typ/ Target	Max	unit
Pixel size		7 x 7		um
Pixel pitch in x direction		7		um
Number of dark pixels in most left segment		2x32		pixels
Fill Factor		100		%
Quantum efficiency at 630nm	50	60	70	%
Full Well capacity(4)	30	46	65	ke-
Total System Gain K		0.076		DN/e-
DSNU rms (1;5)		4	10	DN/12bit
Responsivity (1)		77		DN/nJ/cm2 (@12bit)
Responsvity analogue gain 4x (6)		310		DN/nJ/cm2 (@12bit)
PRNU rms (1;5)		0.7%	3%	% (full scale)
PRNU pp (1; 5)		4%	8%	% (full scale)
ADC Programmable gain	-6		20	dB
ADC gain resolution		8		bit
Blooming overload tolerance	100x	infinite		
Lag		0	0.01	%
Crosstalk (optical & electrical)		2	5	%
Exposure time range	2		infinite	us
Temporal noise Dark rms (2)*		1.5	4	DN/12bit
Dark noise electrons rms (2)*		22		e-
NEE (noise equivalent energy) unity gain (1)		0.02		nJ/cm2
Temporal noise Dark rms gain 4x (6)*		2.9	5	DN/12bit
Dark noise electrons rms gain 4x (6)*		7		e-
NEE (noise equivalent energy) analogue gain x4 (6)*		0.01		nJ/cm2
Non Linearity (3)		2	5	%
Dark current @27C		3	50	e-/ms
Maximum Line Rate 2:1 TDI mode			80	kScan/s
Maximum Line Rate dual line mode			160	kScan/s
ADC Resolution		12 (13)***		bit
Number of output taps		4 for each 2x2k pixels segment		
Configuration Interface		Serial 4 line (1 interface for each line and each 2k segment)		
Integration control**		Asynchronous, with 6 digital signals		
Trigger delay			1	us
Integration & Readout		Interleaved		

(5) Tint=10us, Unity gain (CDS_gain = 0 -> x1; Inverse ADC gain = 0x20h)
(6) T=27ºC , Tint=20us, Unity gain (CDS_gain = 0; -> x1 Inverse ADC gain = 0x20h)

(7) Measured in % deviation from full scale signal for the signal range of 5% - 95% (according to EMVA1288 proposal for linearity measurement)
(8) At unity gain (CDS_gain = 0 -> x1; Inverse ADC gain = 0x20h; end counter 128 (4096 ADC levels))
(5) Ramp offset and ramp gain must be adjusted for all segments to match with each other.

(6) T=27ºC , Tint=20us, Unity gain (CDS_gain = 1; -> x4 Inverse ADC gain = 0x20h)

* {info only: temporal noise can further be reduced by subtracting from each line the average value of the dark reference pixels, which will reduce temporal noise components coupled over the supply at frequencies below the line rate. :end info}
** each line can be triggered individually.
*** internal ADC resolution is 13bit.

3.9 Optical characteristics DR-4k-3.5LCC; DR-8k-3.5; DR-16k-3.6

Parameter	Min	Typ/ Target	Max	unit
Pixel Size x*y		3.5*3.5		um2
Pixel Pitch x		3.5		um
Number of dark & special pixels in most left segment		64		pixels
Fill Factor		100		%
Quantum efficiency at 630nm	50	56	70	%
Full Well capacity(4)	15	23	35	ke-
DSNU rms (1;5)		4	10	DN/12bit
Responsivity (1)		39		DN/nJ/cm2 (@12bit)
Responsivity CDS gain 4x (6)		155		DN/nJ/cm2 (@12bit)
PRNU rms (1;5)		0.8	3	% (full scale)
PRNU pp (1; 5)		4%	10	% (full scale)
ADC Programmable gain	-6		20	dB
ADC gain resolution		8		bit
Blooming overload tolerance	100x	infinite		
Lag		0	0.1	%
Crosstalk (optical & electrical)		2	5	%
Exposure time range	1		infinite	us
Temporal noise Dark rms (2)*		1.6	5	DN/12bit
NEE (noise equivalent energy) unity gain (1)		0.04		nJ/cm2
Temporal noise Dark rms gain 4x (6)*		3.4	6	DN/12bit
NEE (noise equivalent energy) analogue gain x4 (6)		0.02		nJ/cm2
Non Linearity (3)		2	5	%
Maximum Line Rate			80	kScan/s
ADC Resolution		12 (13)***		bit
Number of output taps		4per 4k pixel segment		
Configuration Interface		Serial 4 line 2 Interfaces for each 4k pixel segment		
Integration control		Asynchronous , with 4 digital signals		
Trigger delay			1	us
Integration & Readout		Interleaved		

(1) Tint=10us, Unity gain (CDS_gain = 0 -> x1; ADC ramp = 29)
(2) T=27ºC , Tint=20us, Unity gain (CDS_gain = 0; -> x1 ADC ramp = 29)
(3) Measured in % deviation from full scale signal for the signal range of 5% - 95% (according to EMVA1288 proposal for linearity measurement)
(4) At unity gain (CDS_gain = 0 -> x1; ADC ramp = 29; end counter 128 (4096 ADC levels))

(5) Ramp offset and ramp gain must be adjusted for all segments to match with each other Placement of pixels

(6) T=27ºC , Tint=20us, Unity gain (CDS_gain = 1; -> x4 ADC ramp = 29)

* {info only: temporal noise can further be reduced by subtracting from each line the average value of the dark reference pixels, which will reduce temporal noise components coupled over the supply at frequencies below the line rate. :end info}
*** internal ADC resolution is 13bit.

3.10 Quantum efficiency all B&W versions

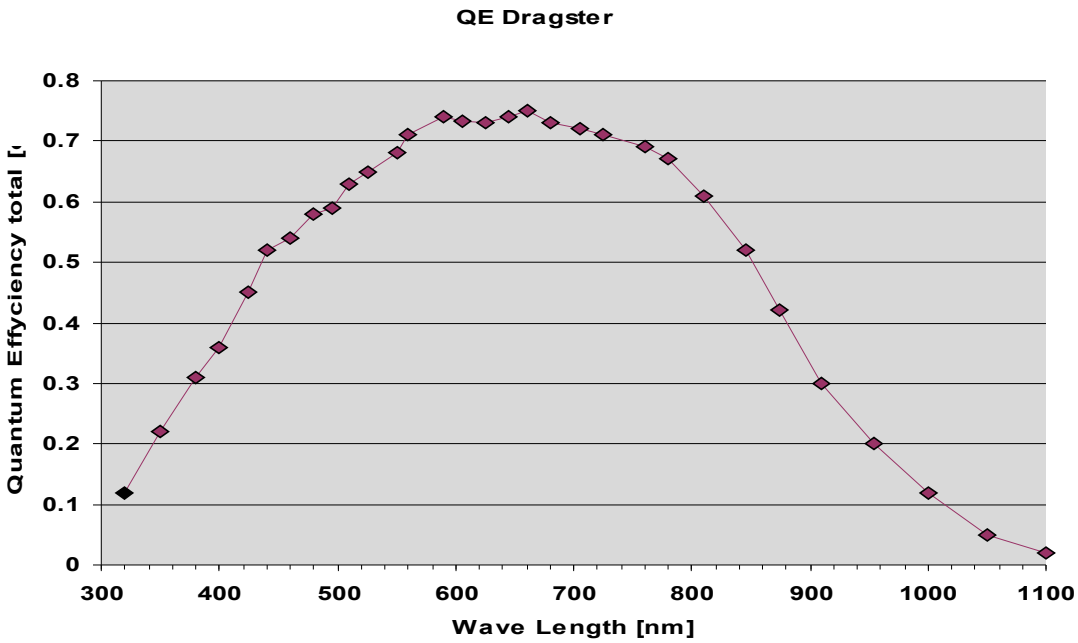


Fig 1: Quantum efficiency measured according EMVA1288 [detected e-/photon]

3.10.1 Filter transmission for RGB Bayer pattern sensor versions

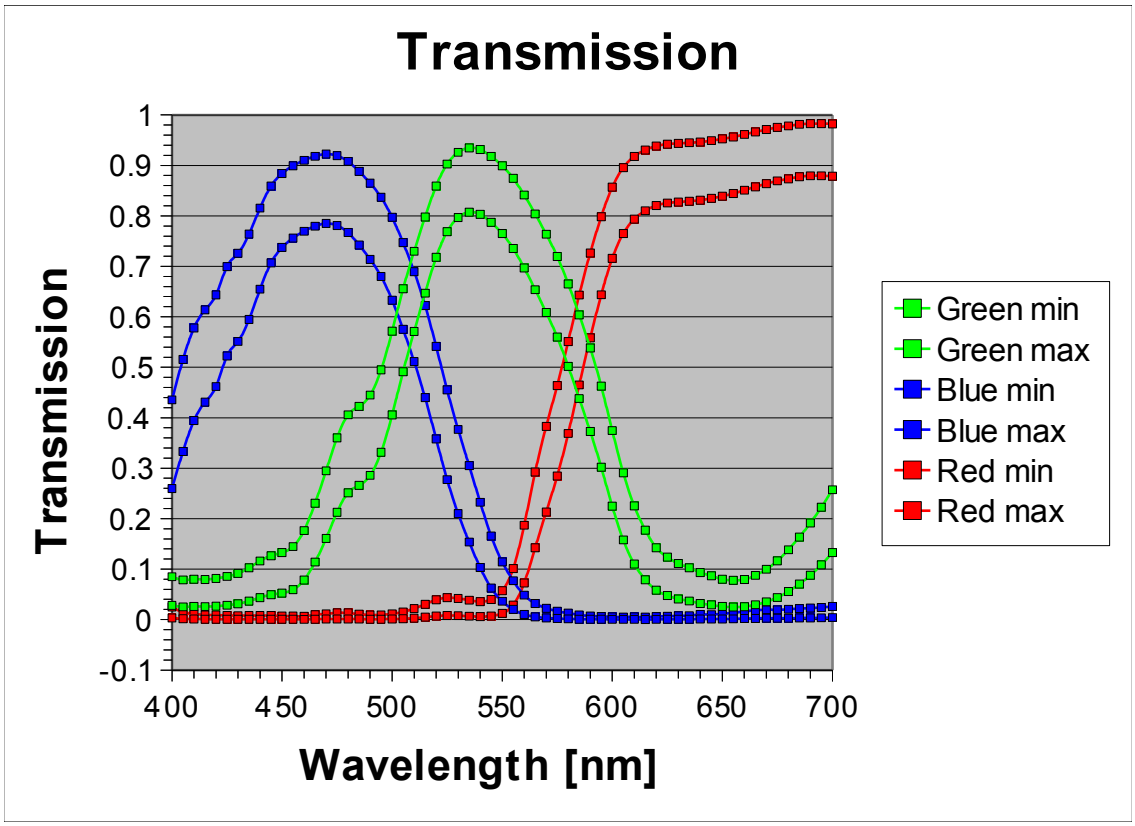


Fig 2: Spectral transmission of colour filters

3.10.2 Color filter arrangement for RGB color filter versions

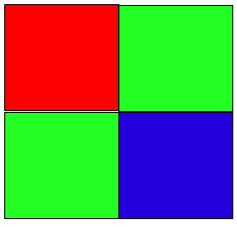


Fig 3: Arrangement of colour filters

3.11 Placement of pixels DR-Xk-7

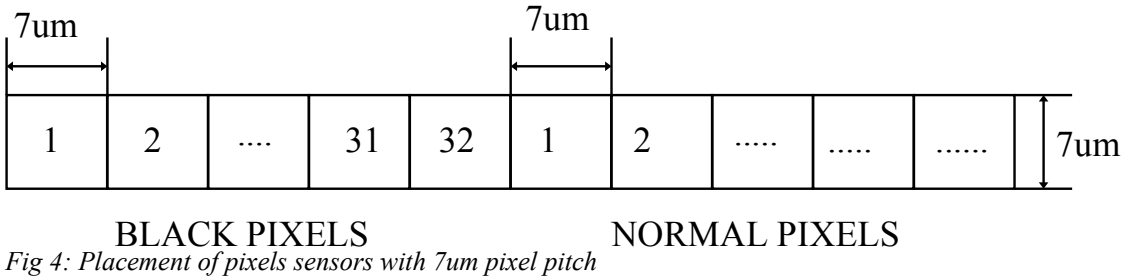


Fig 4: Placement of pixels sensors with 7um pixel pitch

3.11.1 Test & special pixels DR-Xk-7

1. The output from the first pixel is directly connected to the pad 1.*
2. The output from the second pixel is directly connected to the pad 2.*
3. The third pixel is a black pixel, electrically fixed to ADC low saturation
4. The fourth pixels is a white pixel, electrically fixed to ADC high saturation
5. The pixels 5 - 24 are normal pixels however the photo diode is covered by a metal light shield. They serve as a dark reference. However at longer wavelengths the metal shield will not completely shield light any more.
6. The pixels 25 -32 are electrical black pixels. In these pixels the photo diode is disconnected electrically from the readout chain. These pixels will follow all analogue and digital offset variations, however not integrate dark current or any photo current. They can be used check the validity of the dark pixels 5 - 24, or to compensate for line by line ADC offset variations.

* These pixels are light sensitive. The respective outputs are connected to a test point on the head board for debugging purpose in certain package variations.

3.12 Placement of pixels DR-Xk-3.5

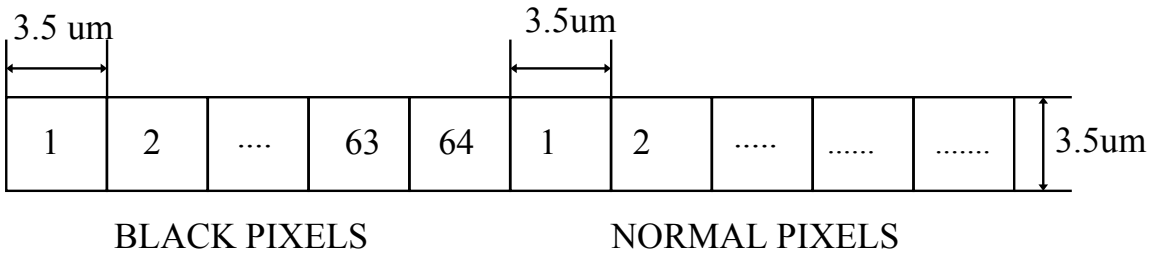


Fig 5: Placement of pixels sensor variations with 3.5um pixel pitch

3.12.1 Test & special pixels DR-Xk-3.5

1. The output from the first & second pixels are directly connected to the pad 1 of the most left segments on top and bottom.*
2. The output from the third and fourth pixels are directly connected to the pad 2of the most left segments on top and bottom.*
3. The fifth and sixth pixels are a black pixel, electrically fixed to ADC low saturation
4. The seventh and eight pixels are white pixel, electrically fixed to ADC high saturation
5. The pixels 9 - 48 are normal pixels however the photo diode is covered by a metal light shield. They serve as a dark reference. However at longer wavelengths the metal shield will not completely shield light any more.
6. The pixels 49 - 64 are electrical black pixels. In these pixels the photo diode is disconnected electrically from the readout chain. These pixels will follow all analogue and digital offset variations, however not integrate dark current or any photo current. They can be used check the validity of the dark pixels 9 - 48, or to compensate for line by line ADC offset variations.

* These pixels are light sensitive. The respective outputs are connected to a test point on the head board for debugging purpose in certain package variations.

4 Functional Description

4.1 General sensor description

Sensors with 3.5um pixels are structurally identical to sensors with 7um pixel. However for the sensor with 3.5um two independent readout blocks are placed, one on tho of the sensor line, which reads out odd pixels and one at the bottom of the sensor line which reads out even pixels. Thus for sensors with 3.5um pixels two independent segments are alway's placed together to form a segment with double resolution compared to the segment with 7um pixel. Thus for sensors with 3.5um pixel all pixel numbers indicated further in this section are double compared to the 7um sensor variations.

The sensor is built of a line of 2080 pixels. The first 32 pixels counting from the left are designated as Black pixels, and are used to have a reference for dark current and signal offsets, the remaining 2048 are the normal pixels, responsible for the image. For readout each 2k segment is completely independent. This can be exploited to align the readout of the light sensitive pixels from each segment. To do so, the readout is started in the most left segment 16 Pixel clock cycles earlier than the more right segments. The individual start of readout for different segments can also be exploited to reduce the required signal bandwidth by sequentially addressing the SRAM blocks of different 2k segments and multiplexing the data lines.

4.2 Serial 4 wire configuration interface

For the access to the internal registers of the sensor, a serial interface with 4 wires is implemented. The interface consists in 4 different lines, one clock line (SCLK), one receive (MOSI) and transmit (MISO) line which are synchronous to each other. The fourth line is the chip select (/CS) and must be low to send/receive data trough the lines. The sensor will be always slave in the application. By the use of the /CS signal the master can activate the serial interface of an individual segment or several segments together. The bus frequency range is from DC to 20MHz, but must always be lower then MCLK/2.

The data is sent from LSB to MSB. The command word has a length of 16 bits and contains the data of the register and the register address. It is possible to write multiple registers consecutively, sending data and address each 16 SCLK. After the last write word the SCLK should be sent for minimum 2 extra clocks, (maximum 4 SCLK) while /CS is still low.

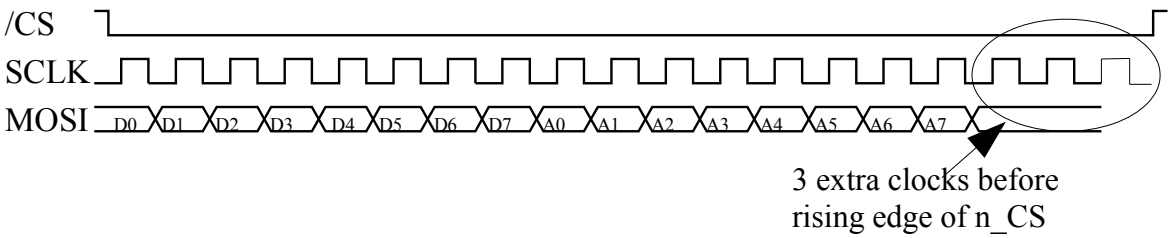
The updating to the registers is performed after update request bit is sent at the next rising edge of "RESET_COUNTER" signal. The last word sent to the registers has to be always to register 0x01 and containing the update request bit, otherwise not update is performed.

Writing Operation

The writing operation is performed by sending the word containing the data and the address, no acknowledge signal or indication is given back.

Time 0 Time 16SCLK

LSB ..... ***MSB***	
<---------- 16 bit of serial data ---------->	
<---------- Data ---------->	<---------- Address ---------->
D0 | D1 |..... ..... D6 | D7	A0 | A1 | .... A6 | A7

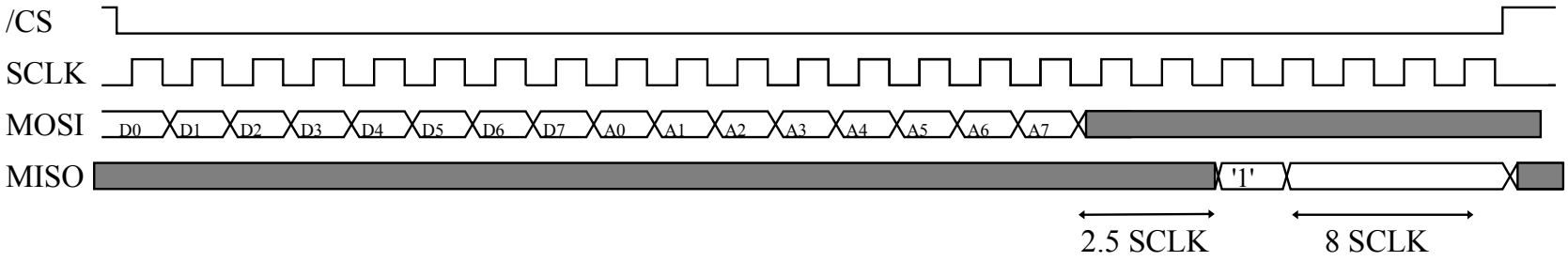


Reading Operation

To perform a read operation, the address for the register to be read, has to be written on register 15 (as data). The output data will be sent over the MISO line, with one leading one, and with 2 SCLK delay to the last bit of the address word (LSB first).

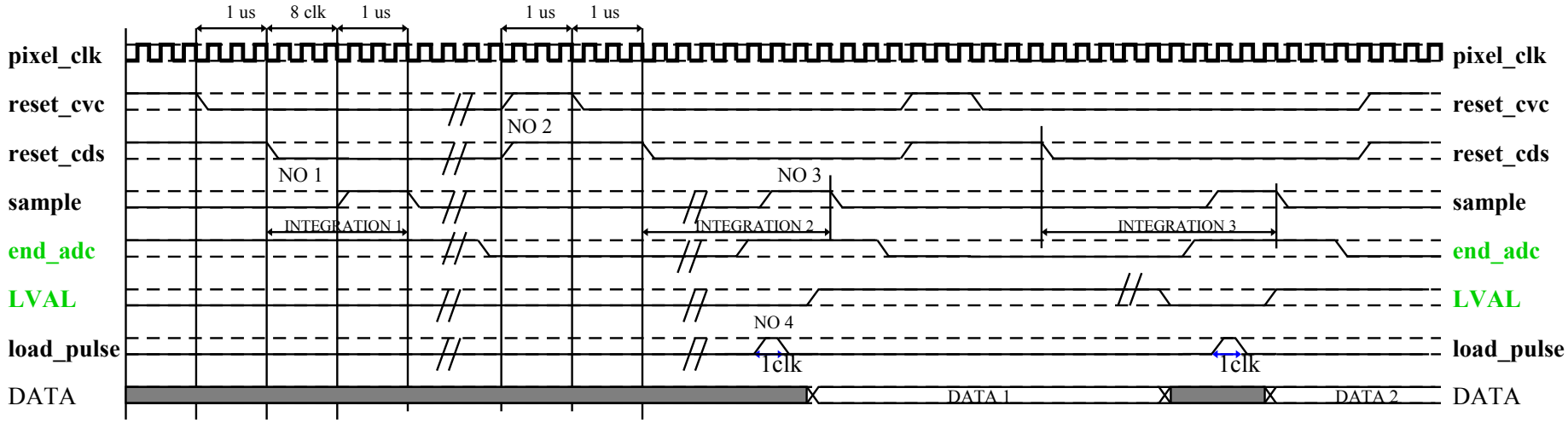
Time 0 Time 16SCLK

LSB ..... ***MSB***	
<---------- 16 bit of serial data ---------->	
<-------- Data (read address) ---------->	<---------- Address R15 ---------->
D0 | D1 |..... D6 | D7	A0 | A1 | ..... A6 | A7



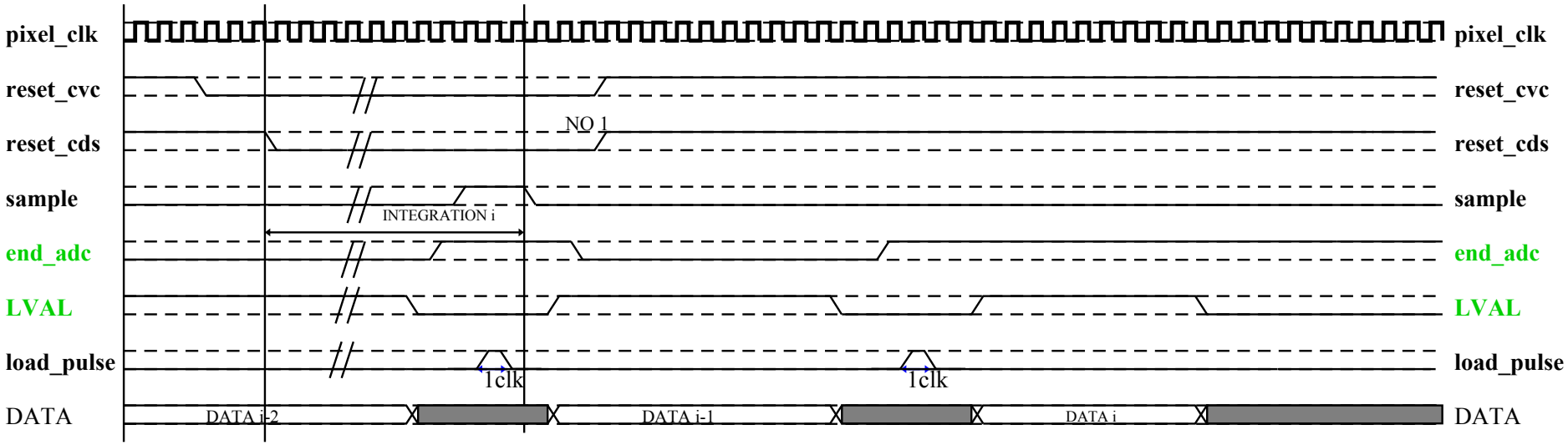
4.3 Timing diagrams

Start of integration



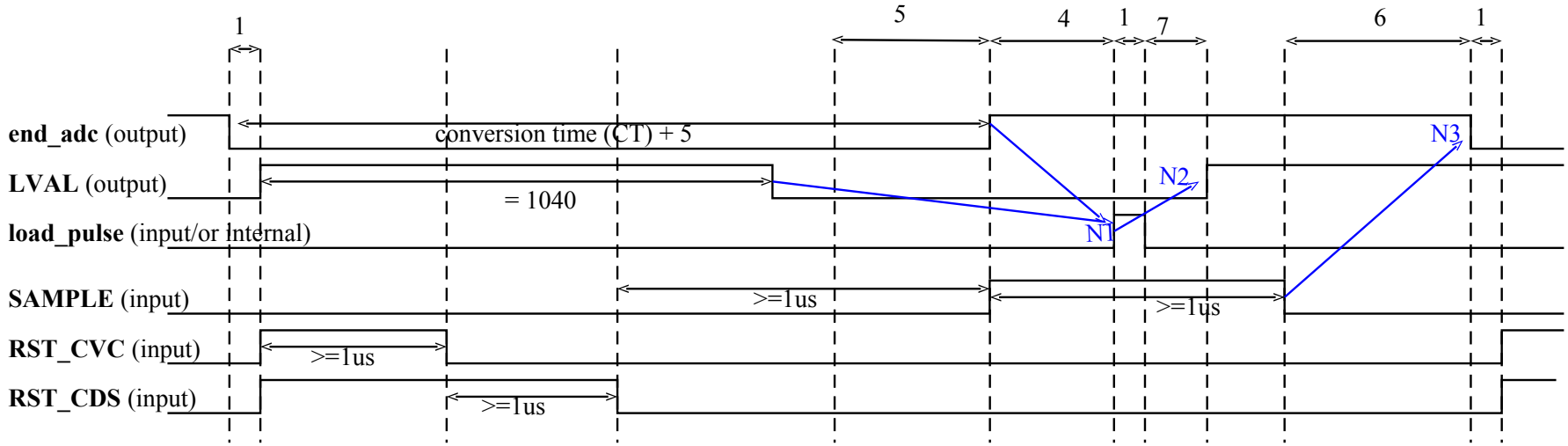
NO 1 - To start the integration the user should send the falling edge of RST_CVC and RST_CDS with a delay of 1us, but no less delay than 8 clks the user should send the raising edge of SAMPLE. However the rising edge of SAMPLE should never be sent before the end of the active ADC conversion. (END_ADC = HIGH)
NO 2 - The user can send the rising edge of RST_CVC and RST_CDS only 6clk after falling edge of sample. (Note 6clk after falling edge of sample, END_ADC will have it's falling edge)
NO 3 - The raising edge of SAMPLE should only be sent if END_ADC is HIGH
NO 4 - The load pulse should be sent, with 4 clocks delayed to the latest event, falling edge of LVAL or rising edge of END_ADC.

End of readout entering idle



NO 1 - To put the sensor in idle mode, the user should send the rising edge of RST_CVC and RST CDS, and keep the signal at HIGH Level

Detail end of integration start ADC and readout:



NOTE 1:rising of load = the later of (rising edge end_adc; falling edge LVAL) + 4
NOTE 2: rising of LVAL = rising edge of load_pulse + 8
NOTE 3:falling of end_adc = falling edge of SAMPLE + 6

Conversion time:
if ADC_mode_bit =0)
CT = end_range*32
else (ADC_mode_bit = 1)
CT = [thr1+ (thr2-thr1)/2 + (thr3-thr2)/4 + (end_range -thr3)/8]*32

4.4 Tap organization

4.4.1 Tap organization DR-2k-7

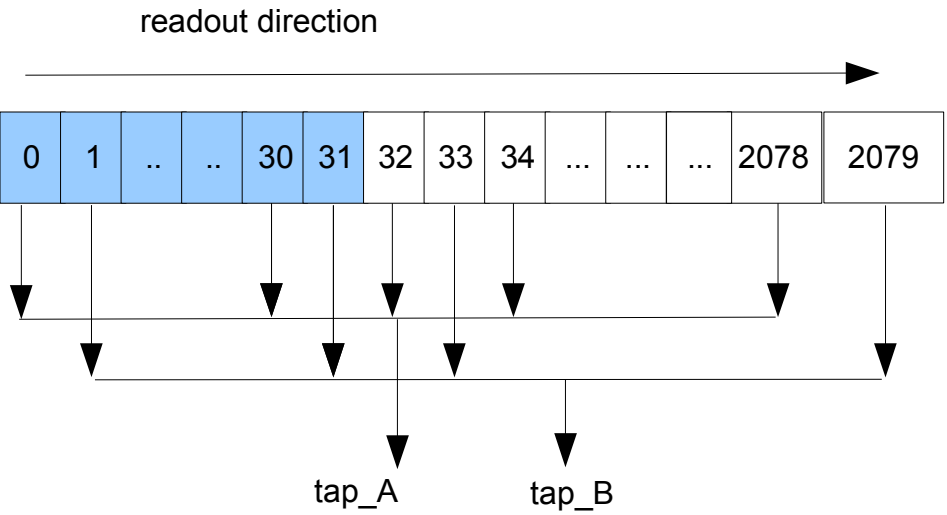


Fig 6: Tap organization DR-2k-7

4.4.2 Tap organization DR-4k-3.5

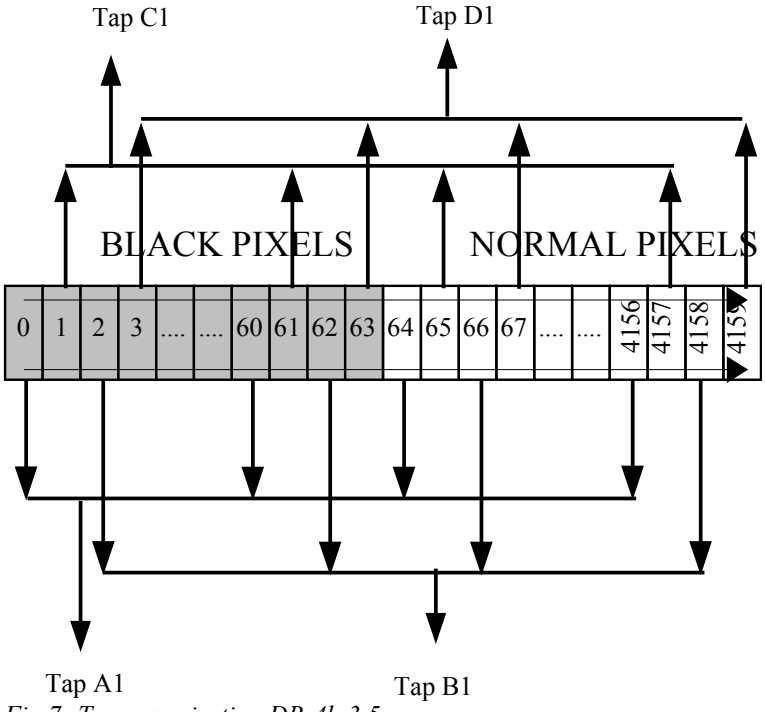


Fig 7: Tap organization DR-4k-3.5

4.4.3 Tap organization DR-2x2k-7

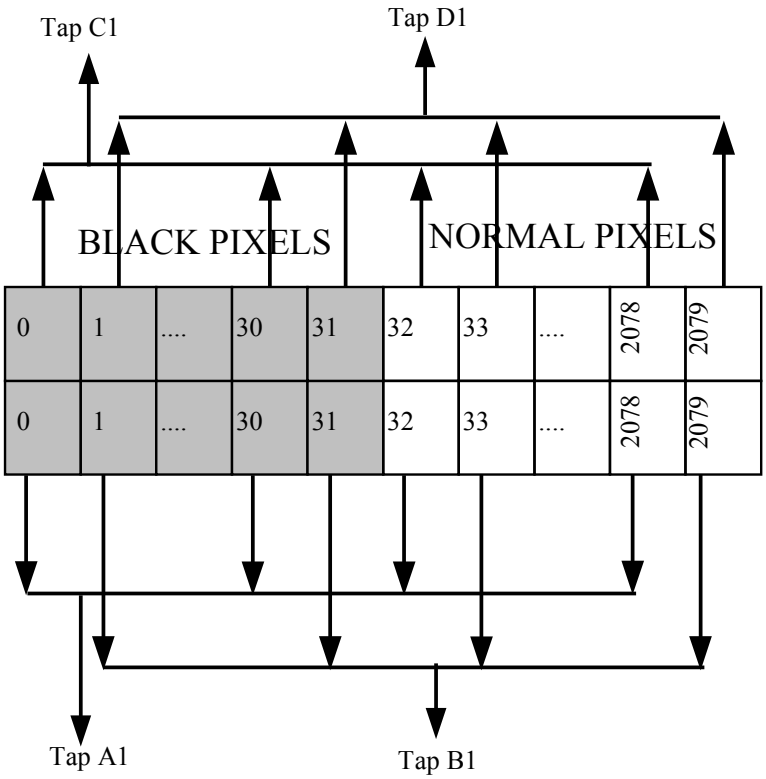


Fig 8: Tap assignment DR-2x2k-7

4.4.4 Tap organization DR-4k-7

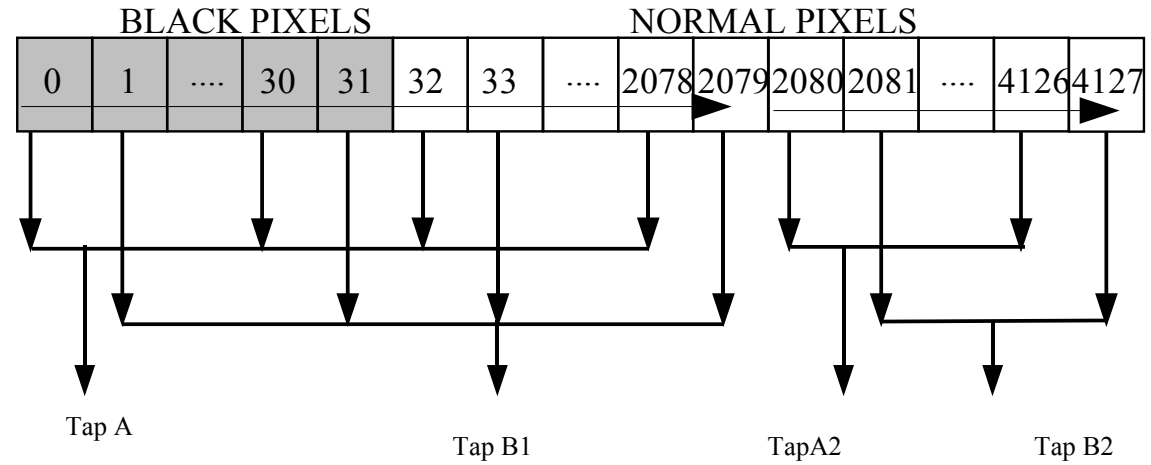


Fig 9: Tap organization DR-4k-7

4.4.5 Tap organization DR-8k-3.5

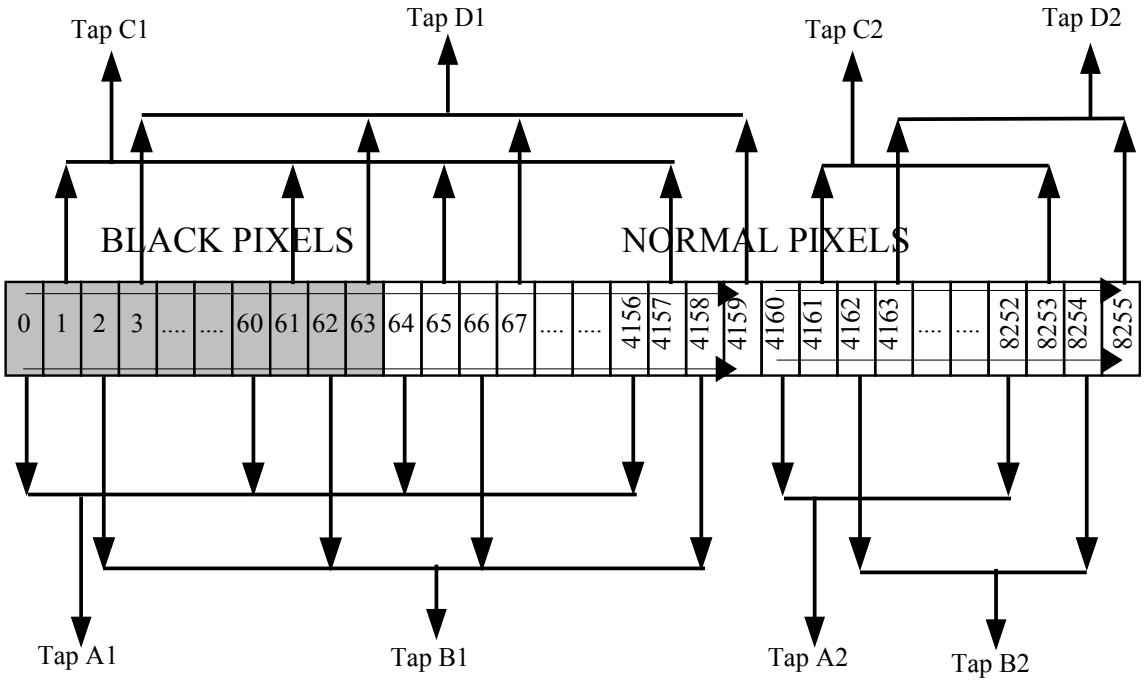


Fig 10: Tap organization DR-8k-3.5

4.4.6 Tap organization DR-2x4k-7

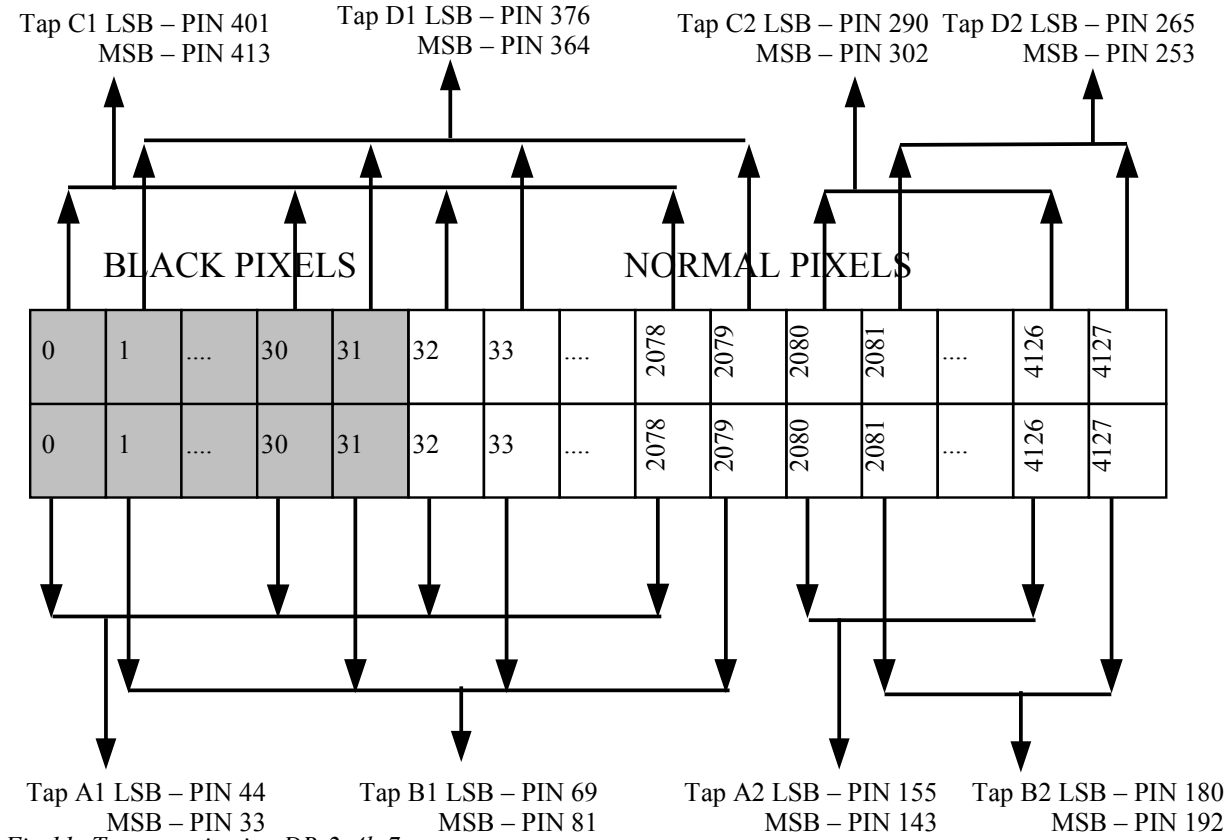


Fig 11: Tap organization DR-2x4k-7

4.4.7 Tap organization DR-8k-7

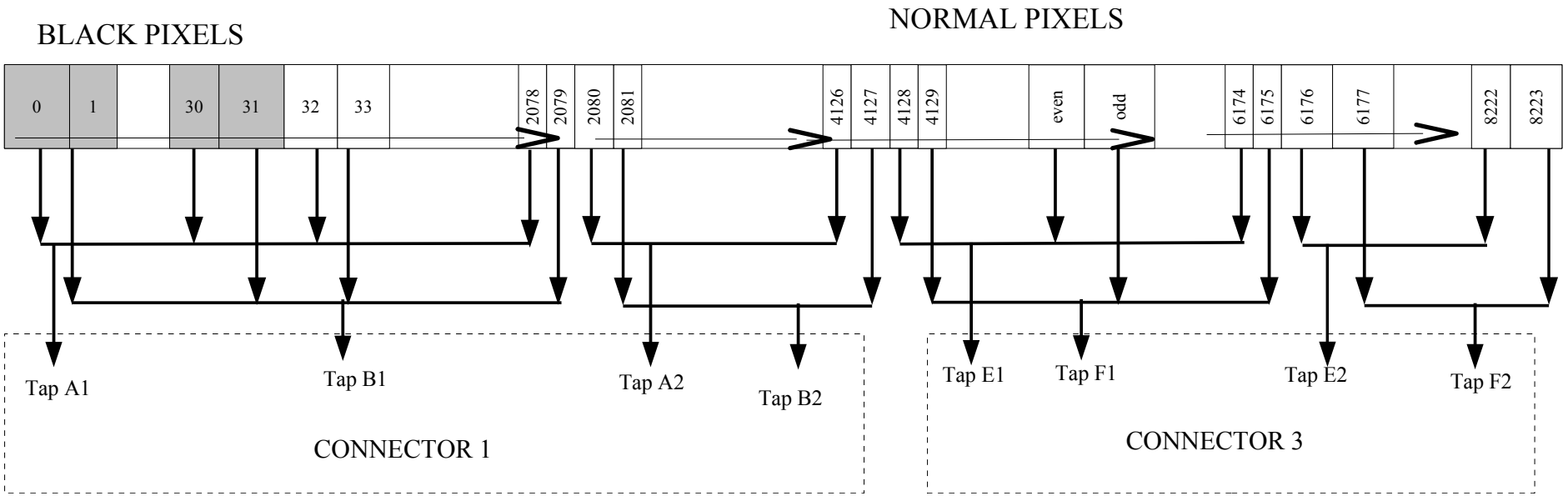


Fig 12: Tap organization DR-8k-7

4.4.8 Tap organization DR-16k-3.5

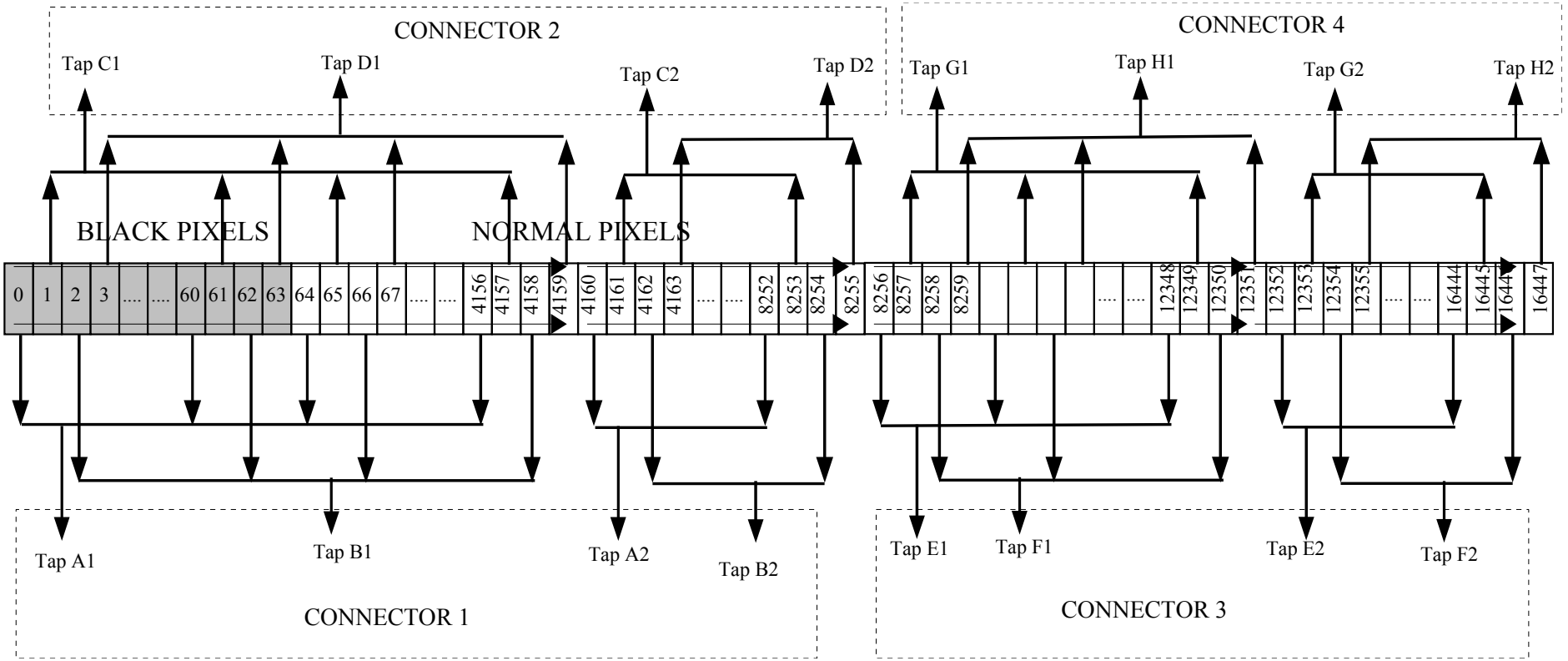


Fig 13: Tap Organization DR-16k-3.5

4.4.9 Tap organization DR-2x8k-7

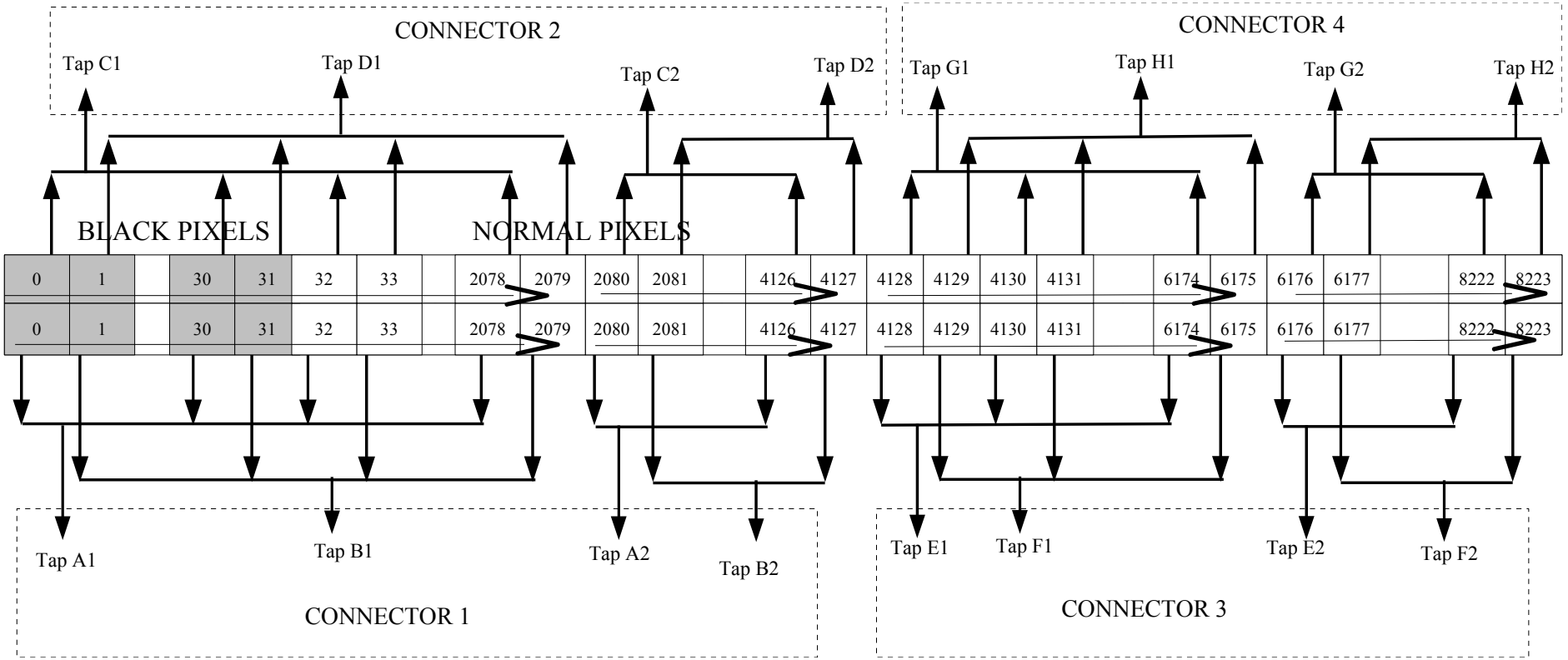


Fig 14: Tap Organization DR-2x8k-7

5 Mechanical Descriptions

DRAGSTER sensors are supplied as COB (chip on board) part with "Invar" enforcement. This package provides easy integration in a camera, precise mechanical alignment and prevents any alteration of the sensors Z-position due to temperature effects. Default delivery form is with a cover glass. Optional the sensor can be delivered without cover glass and a globe top protection of the bond wires. Upon request other delivery forms are possible. (Bare die, CSP etc...) Do contact AWAIBA if you require a custom package solutions.

5.1 Package drawings DR-4k-7

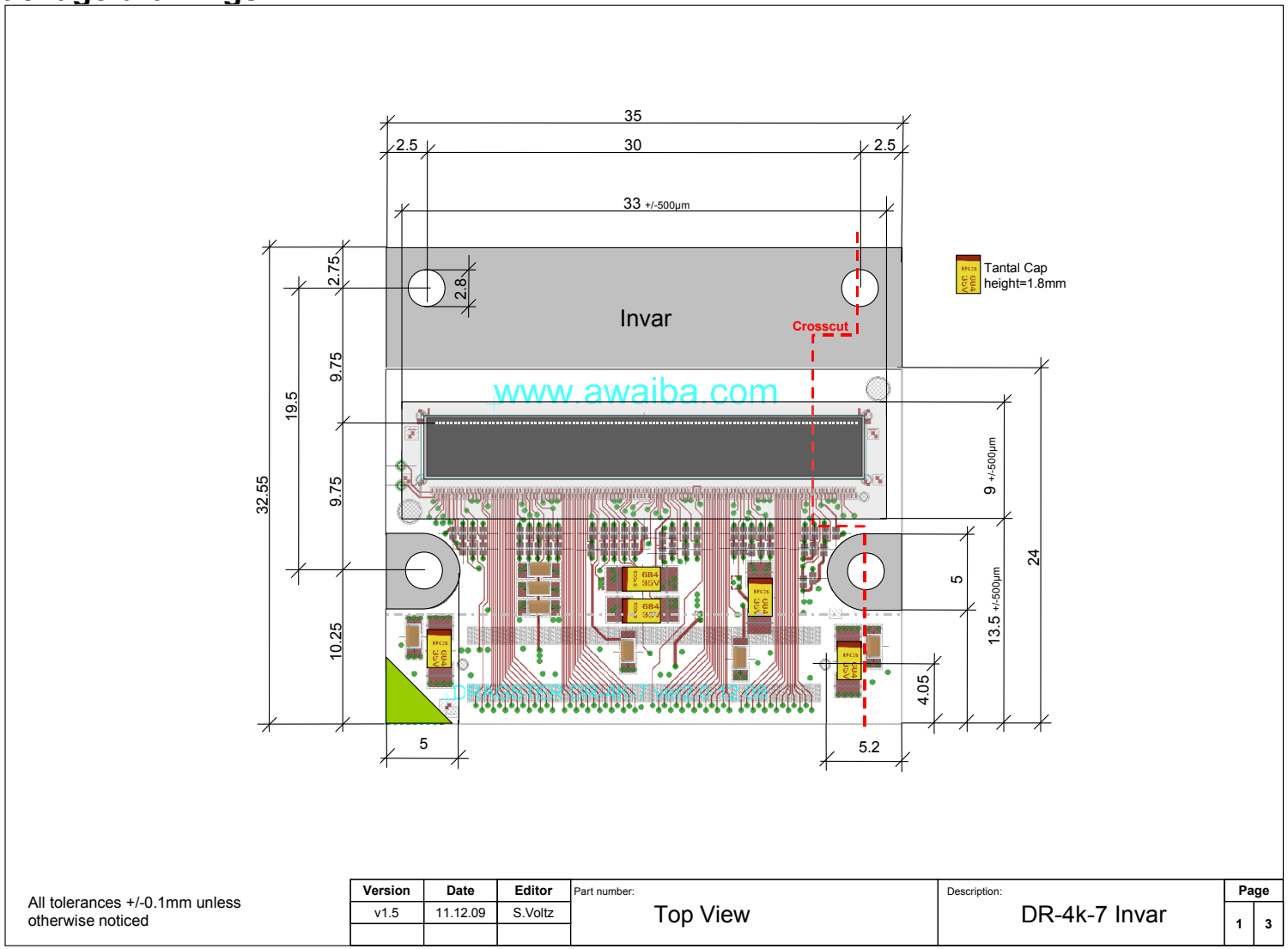


Fig 15: Top view DR-4k-7

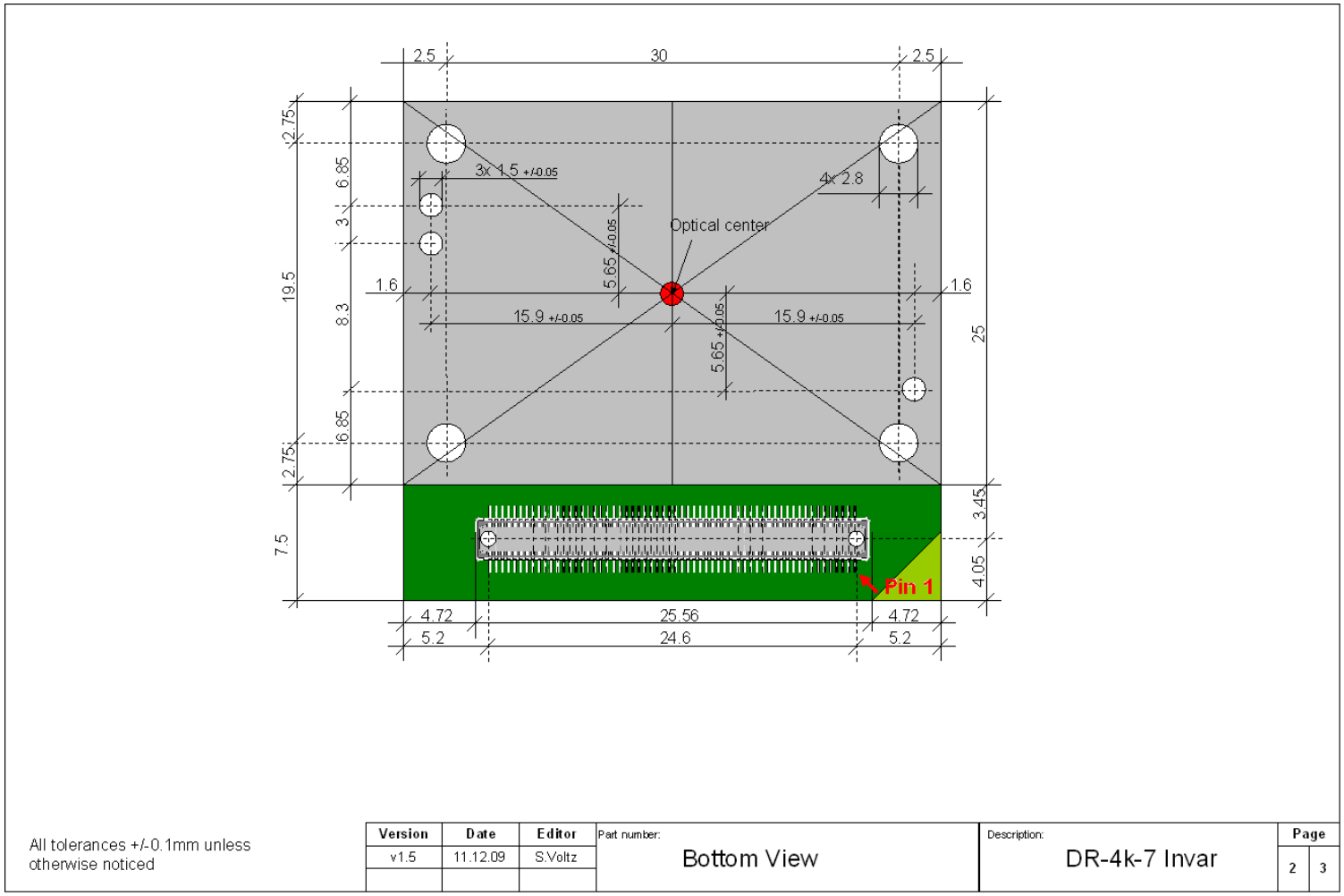


Fig 16: Bottom view DR-4k-7

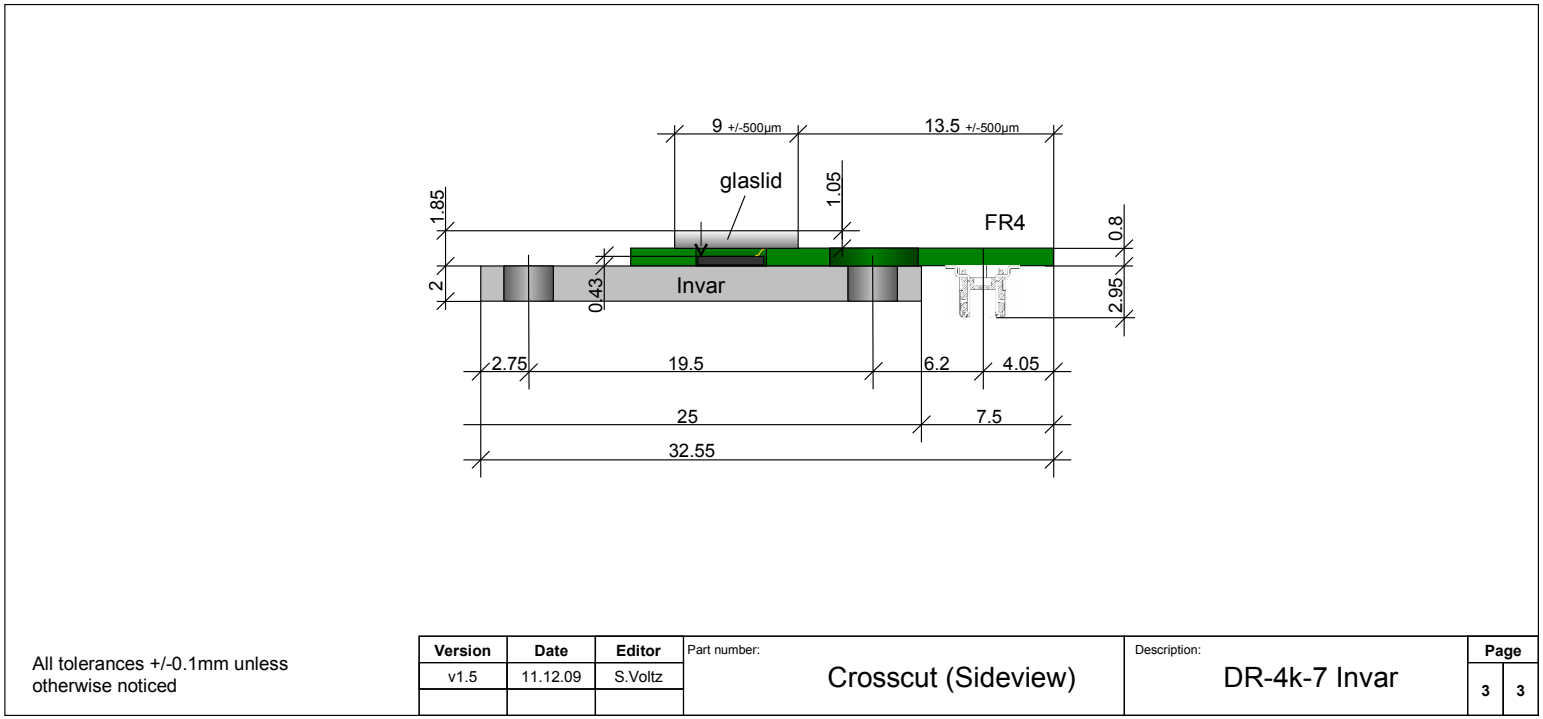


Fig 17: Side view DR-4k-7

5.2 Package drawing DR-8k-7

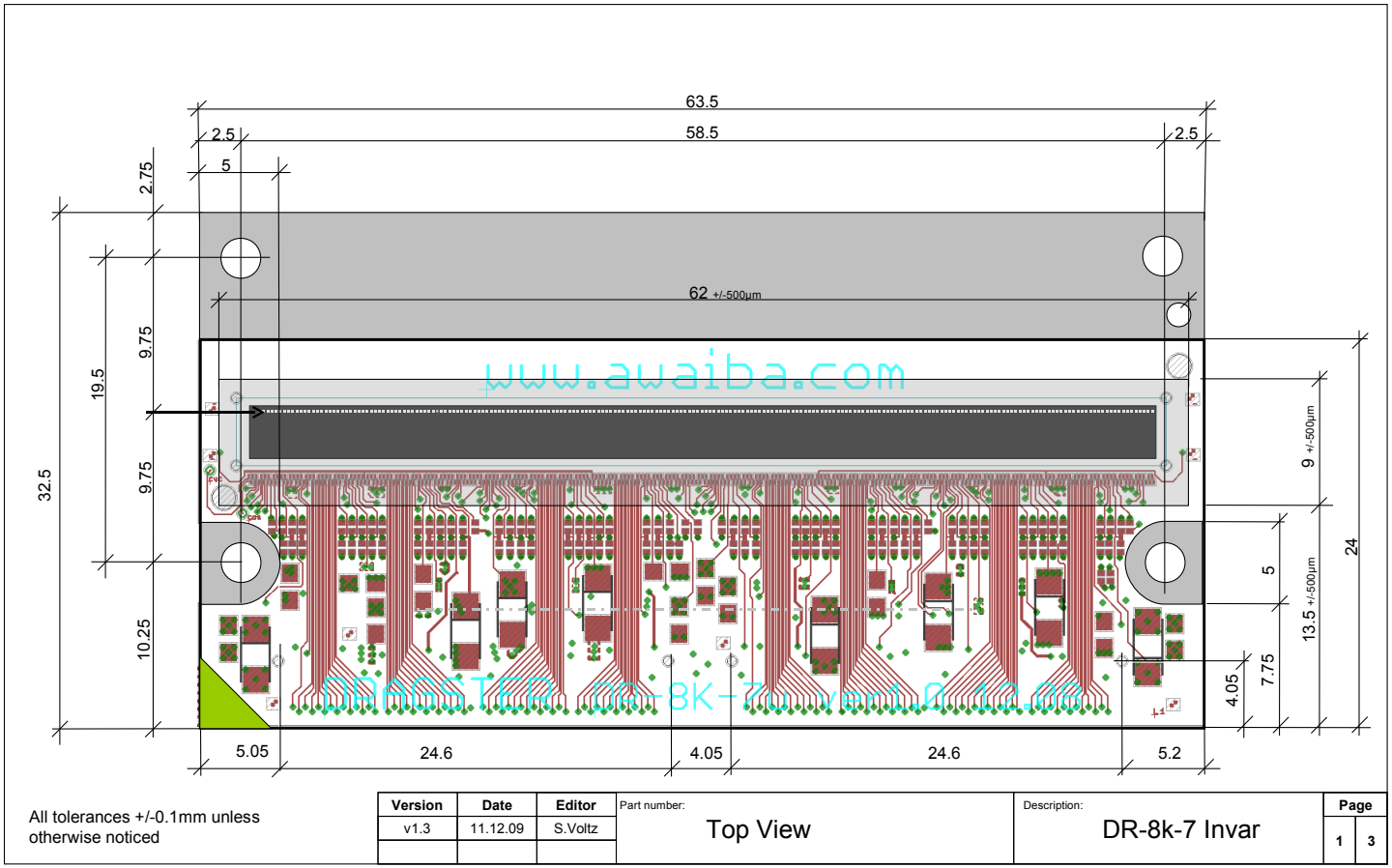


Fig 18: Top view DR-8k-7

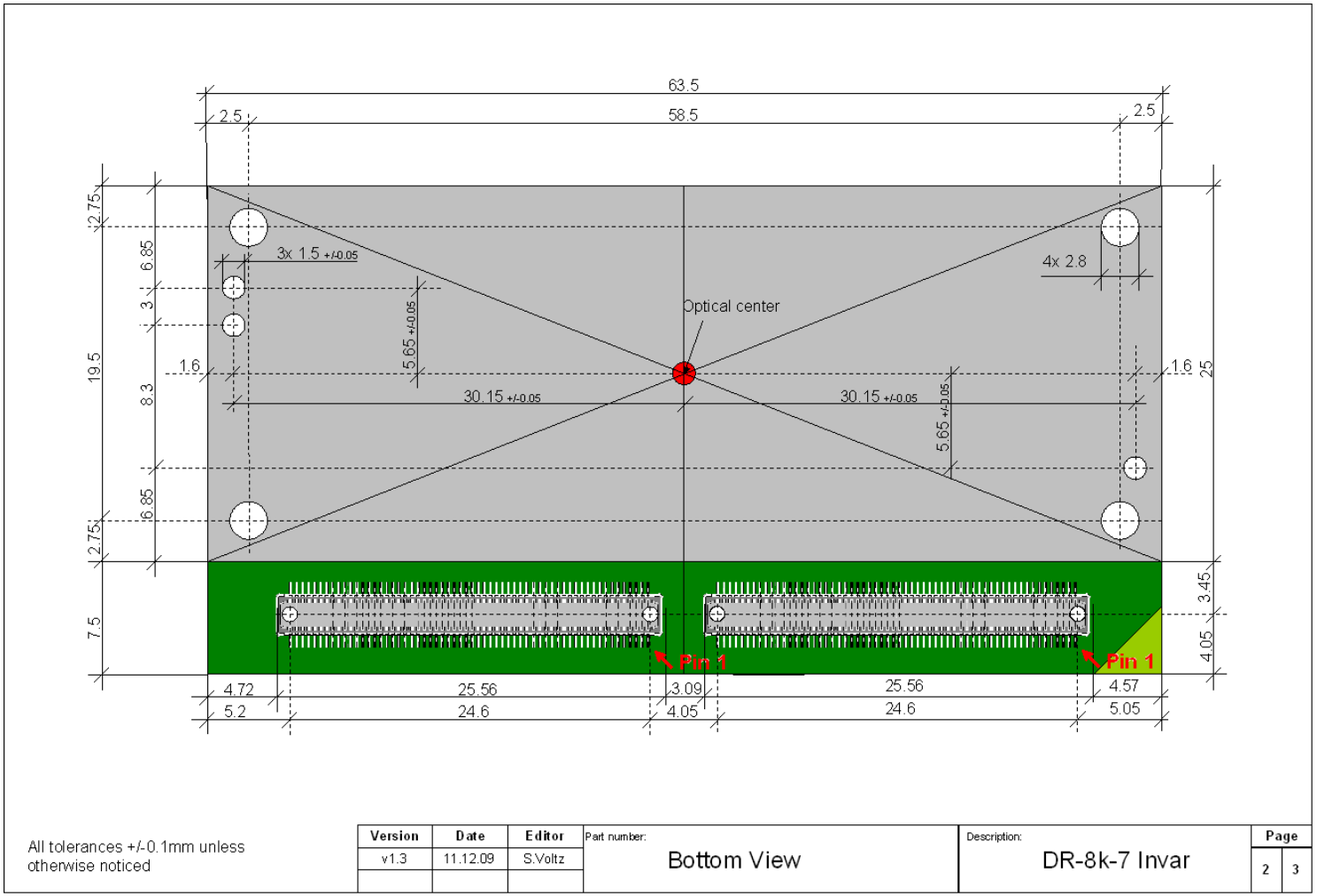
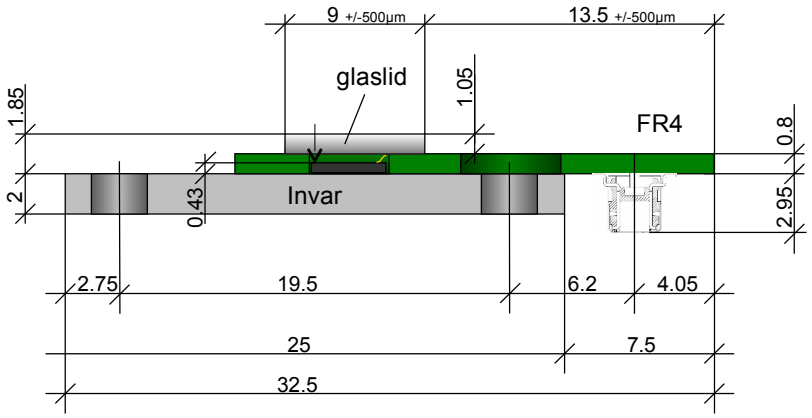


Fig 19: Bottom view DR-8k-7



All tolerances +/-0.1mm unless otherwise noticed

Version	Date	Editor	Part number:	Description:	Page	
v1.3	11.12.09	S.Voltz	Crosscut (Sideview)	DR-8k-7 Invar	3	3

Fig 20: Side view DR-8k-7

5.3 Package Drawing DR-2x2k-7-invar & DR-4k-3.5-invar

all physical outlines of DR-2x2k-7-invar and DR-4k-3.5-invar are identical to the physical outlines of the DR-8k-3.5 package drawing.

5.4 Package Drawing DR-8k-3.5 & DR-2x4k-7

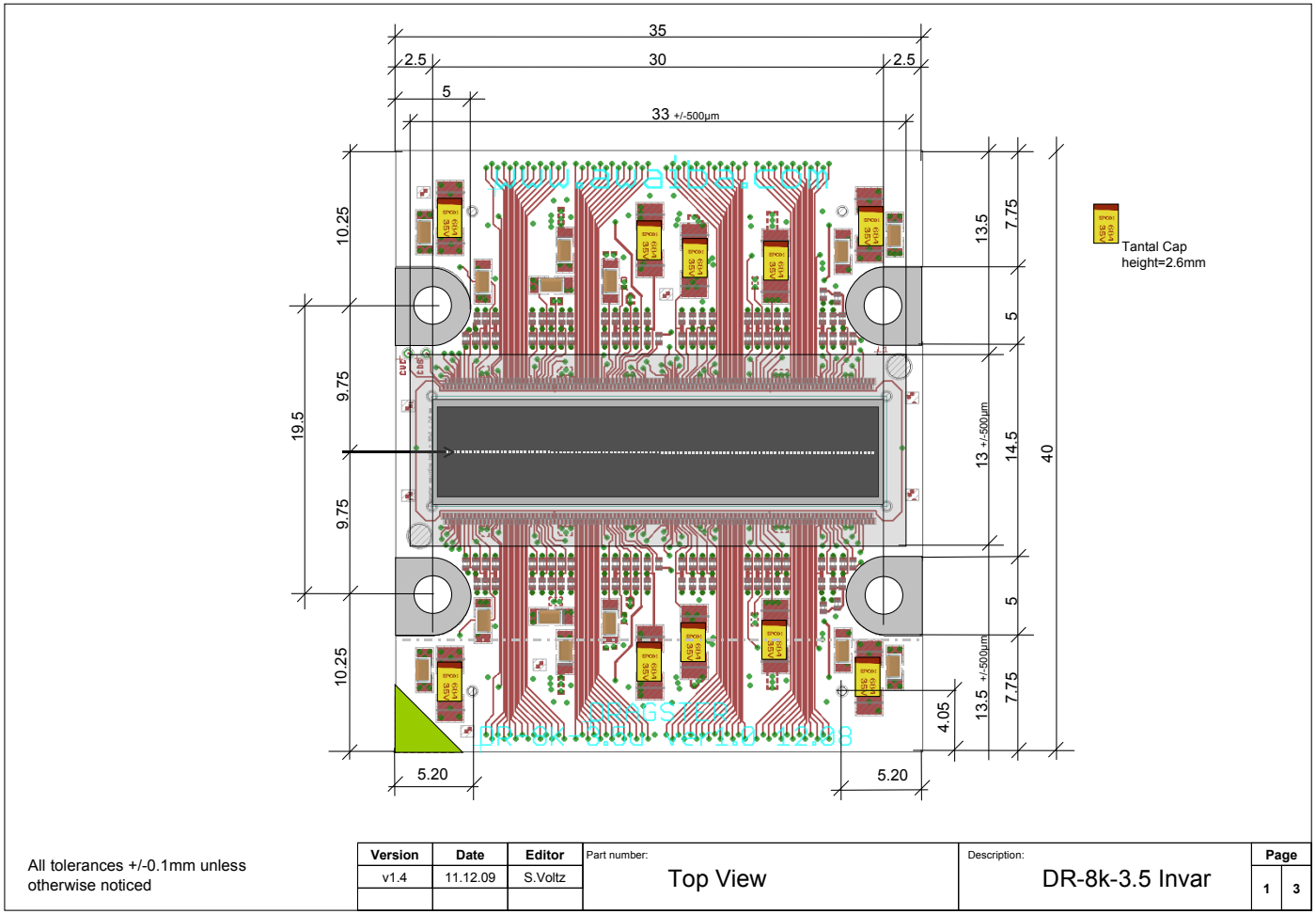


Fig 21: Top view DR-8k-3.5 & DR-2x4k-7

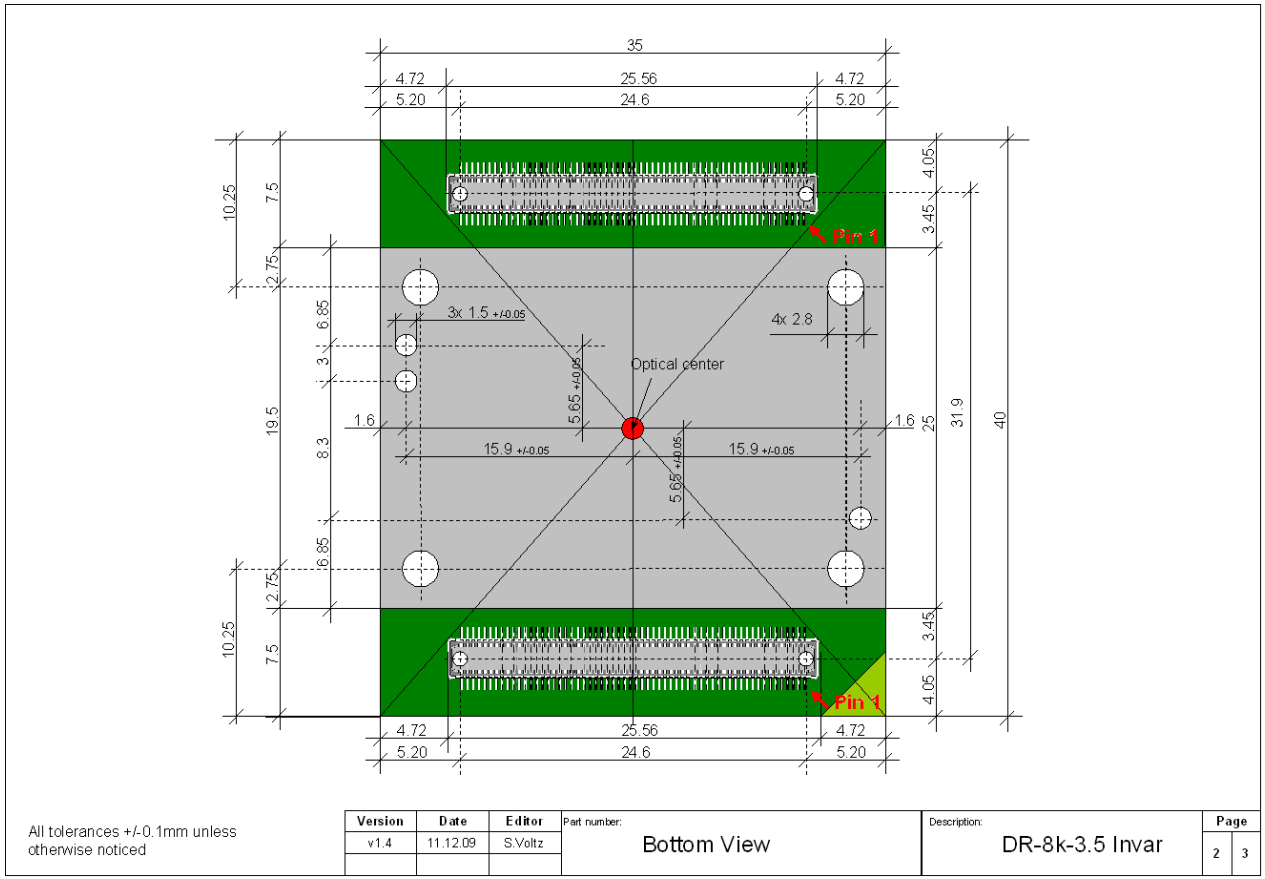
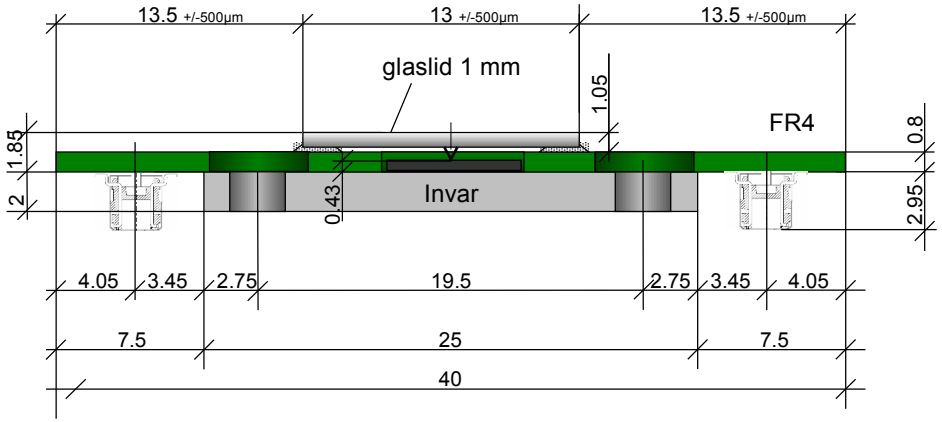


Fig 22: Bottom view DR-8k-3.5& DR-2x4k-7



All tolerances +/-0.1mm unless otherwise noticed

Version	Date	Editor	Part number:	Description:	Page
v1.4	11.12.09	S.Voltz	Crosscut (Sideview)	DR-8k-3.5 Invar	3 3

Fig 23: Side view DR-8k-3.5 & DR-2x4k-7

5.5 Package drawing DR-16k-3.5 & DR-2x8k-7

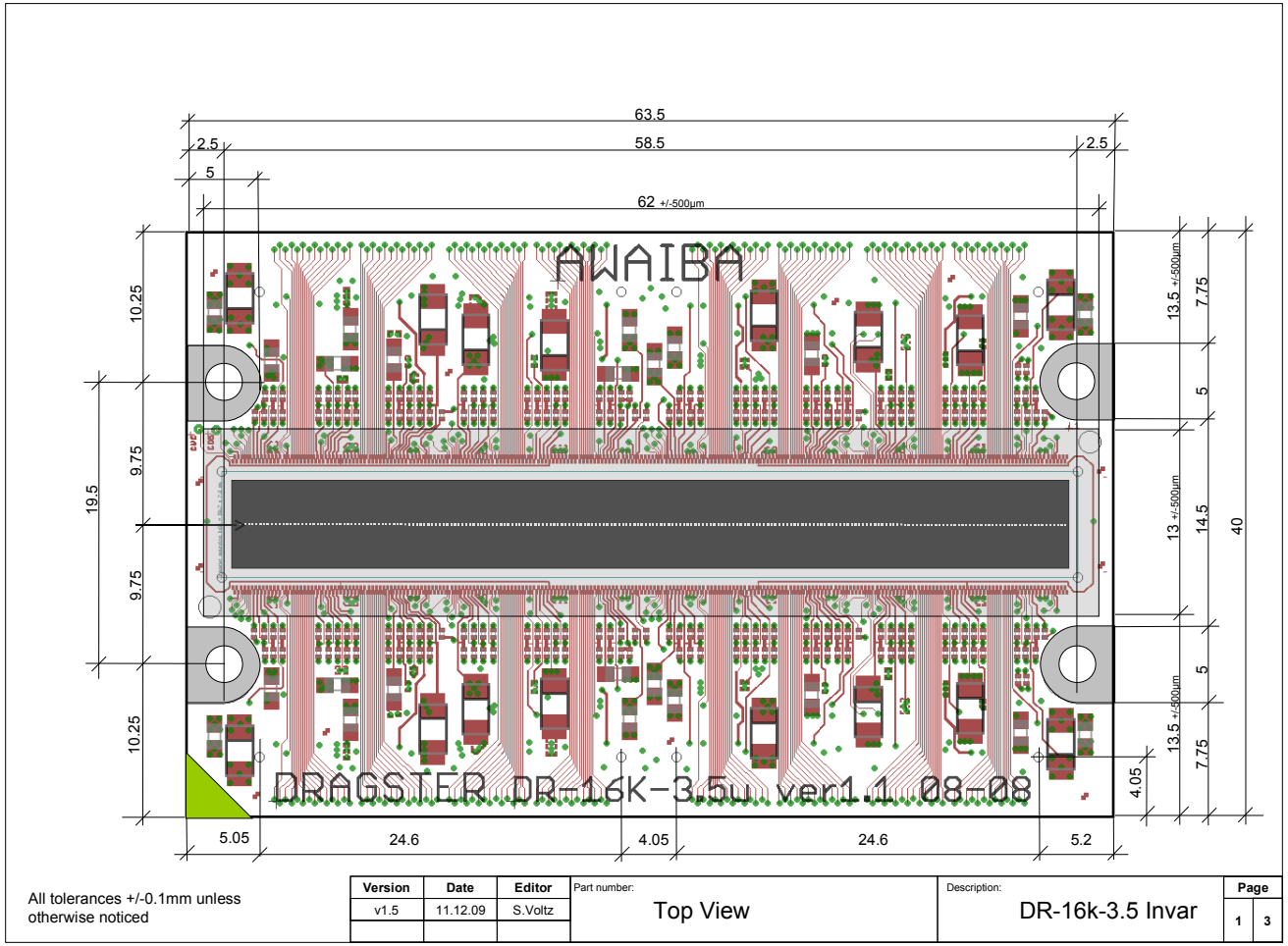


Fig 24: Top view DR-16k-3.5 & DR-2x8k-7

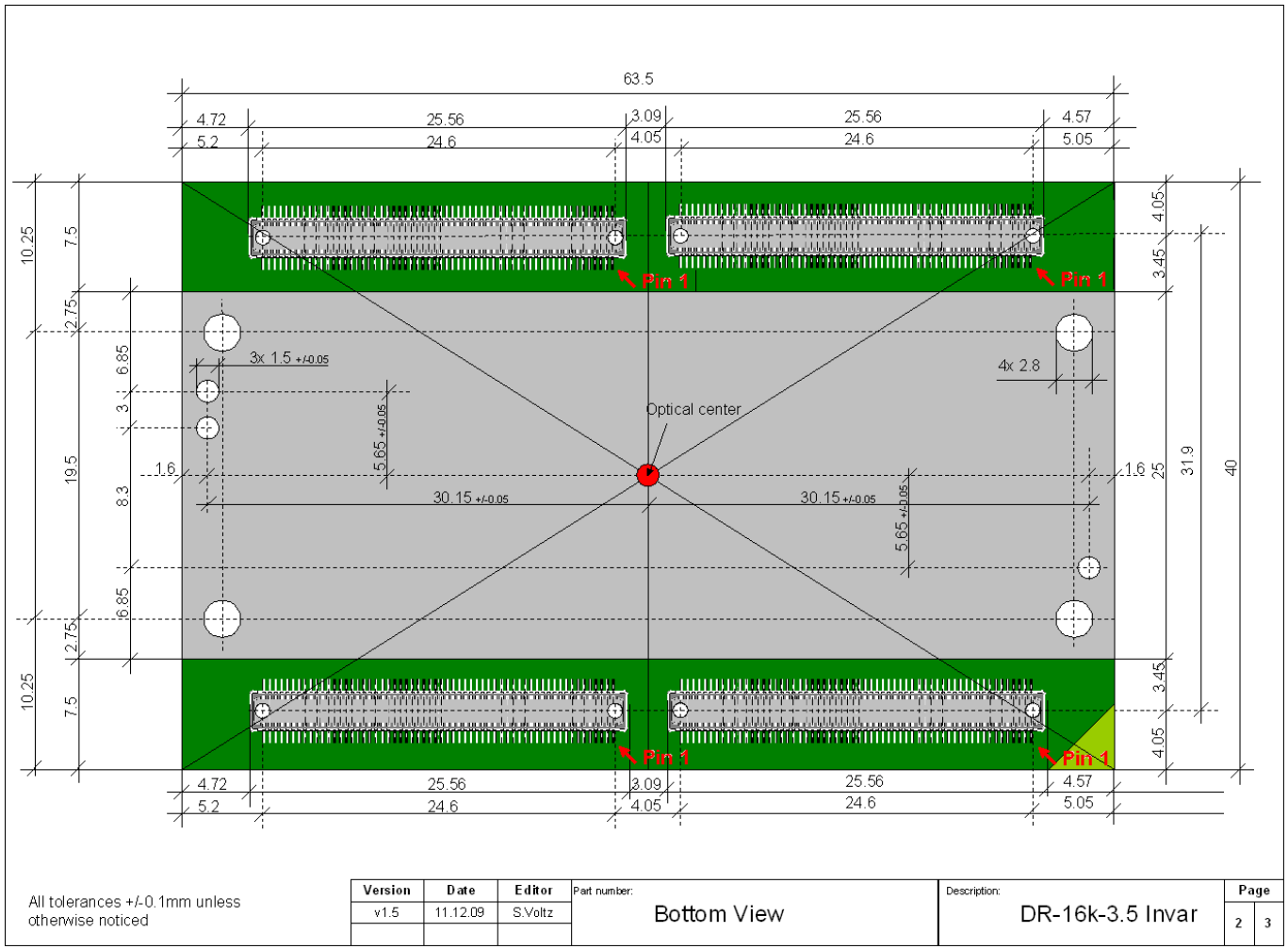
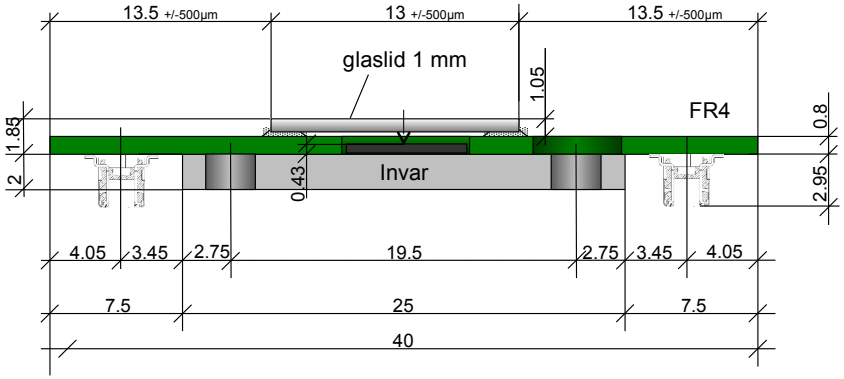


Fig 25: Bottom view DR-16k-3.5 & DR-2x8k-7



All tolerances +/-0.1mm unless otherwise noticed

Version	Date	Editor	Part number:	Description:	Page
v1.5	11.12.09	S.Voltz	Crosscut (Sideview)	DR-16k-3.5 Invar	3 / 3

Fig 26: Side view DR-16k-3.5 & DR-2x8k-7

5.6 Package drawing DR-2k-7LCC, DR-2x2k-7LCC and DR-4k-3.5LCC

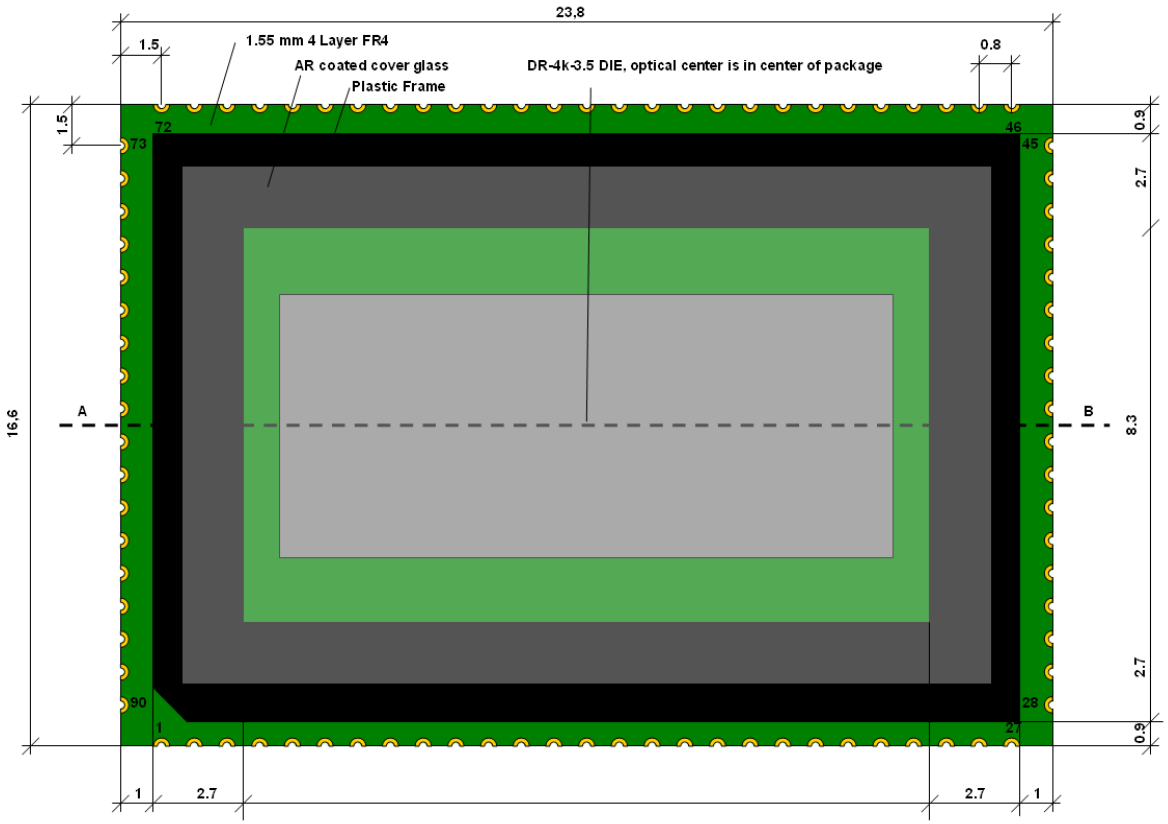


Fig 27: Top view DR-2k-7LCC DR-2x2k-7LCC and DR-4k-3.5LCC

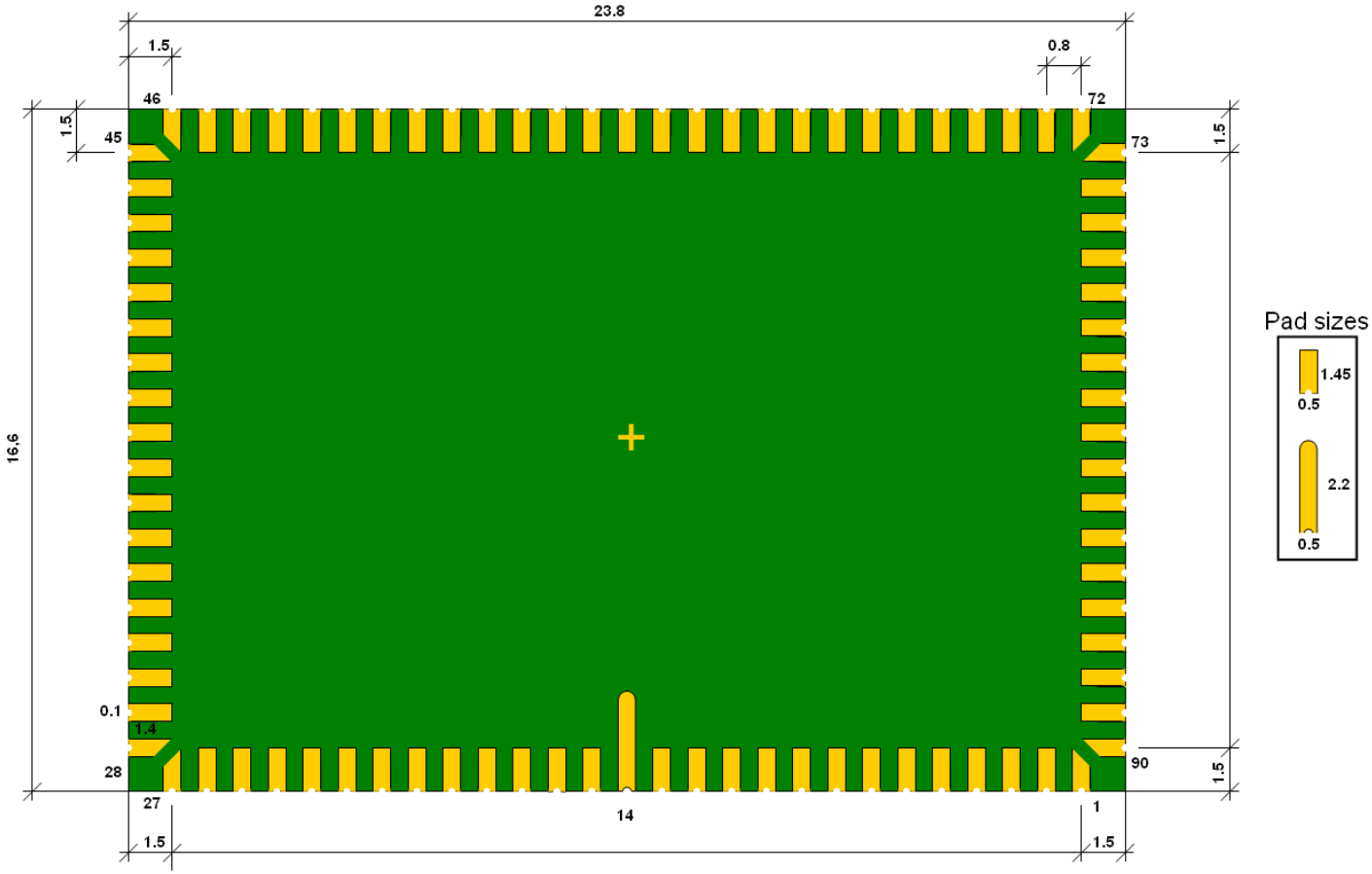


Fig 28: Bottom view DR-2k-7LCC ; DR-2x2k-7LCC and DR-4k-3.5LCC

Fig 29: Side view and cross cut DR-2k-7LCC, DR-2x2k-7LCC and DR-4k-3.5LCC

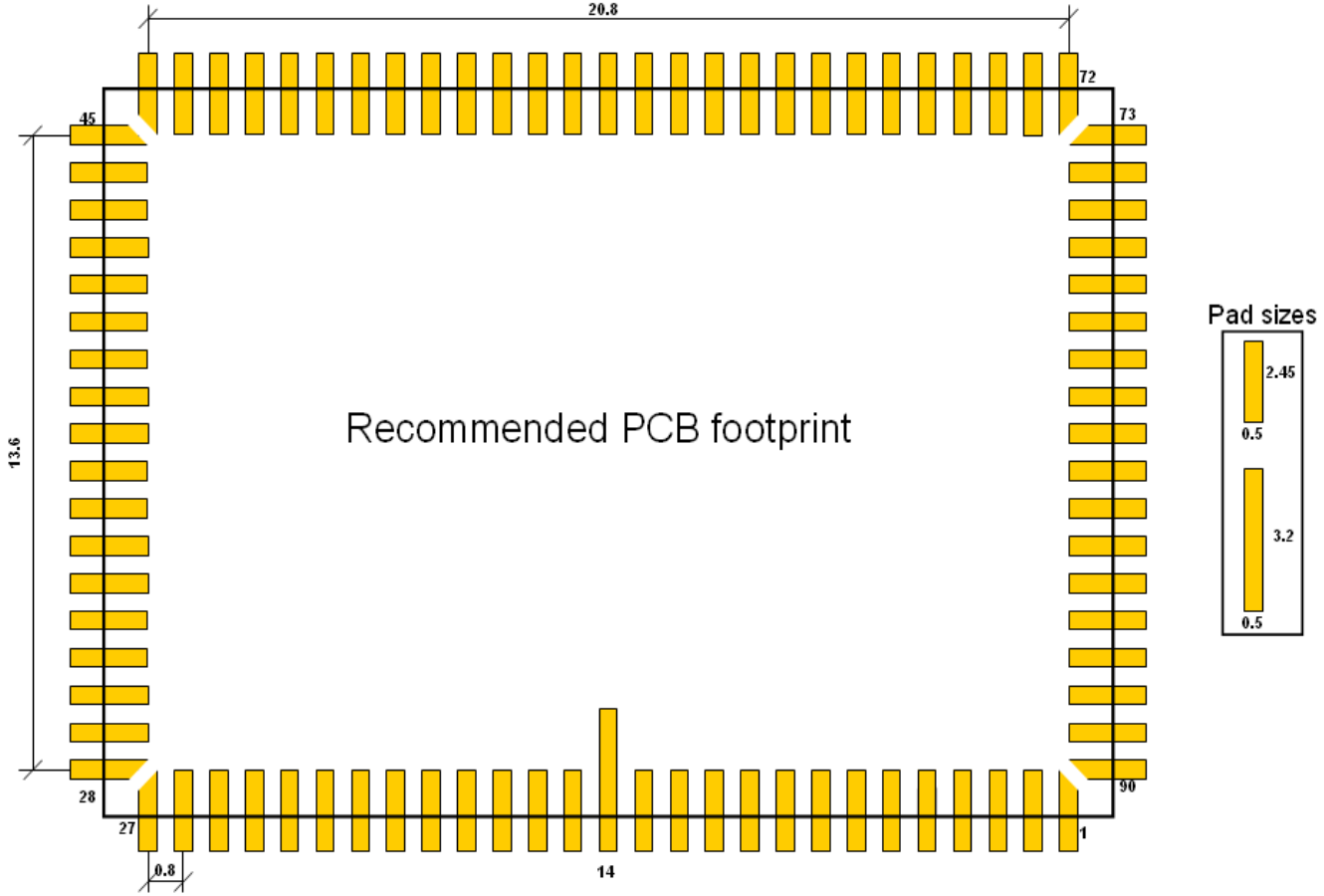


Fig 30: Side view and cross cut DR-2k-7LCC, DR-2x2k-7LCC and DR-4k-3.5LCC

6 Pin outs

6.1 Pinout DR-2k-7LCC, DR-2x2k-7LCC and DR-4k-3.5LCC

Pin	Signal Name DR-4k-3.5LCC & DR-2x2k-7LCC	Signal Name DR-2k-7LCC	Type
1	Tap A1 Bit 11	Tap A1 Bit 11	Digital Output
2	Tap A1 Bit 9	Tap A1 Bit 9	Digital Output
3	Tap A1 Bit 7	Tap A1 Bit 7	Digital Output
4	Tap A1 Bit 5	Tap A1 Bit 5	Digital Output
5	Tap A1 Bit 3	Tap A1 Bit 3	Digital Output
6	Tap A1 Bit 1	Tap A1 Bit 1	Digital Output
7	VSS	VSS	Ground
8	LVAL Tap A1/B1	LVAL Tap A1/B1	Digital Output
9	Tap A1 Bit 12	Tap A1 Bit 12	Digital Output
10	Tap A1 Bit 10	Tap A1 Bit 10	Digital Output
11	Tap A1 Bit 8	Tap A1 Bit 8	Digital Output
12	Tap A1 Bit 6	Tap A1 Bit 6	Digital Output
13	Tap A1 Bit 4	Tap A1 Bit 4	Digital Output
14	Tap A1 Bit 2	Tap A1 Bit 2	Digital Output
14	Tap A1 Bit 0	Tap A1 Bit 0	Digital Output
16	Pixel_CLK_Tap A1/B1	Pixel_CLK_Tap A1/B1	Digital Output
17	END_ADC_TAP A1/B1	END_ADC_TAP A1/B1	Digital Output
18	VSS	VSS	Ground
19	Tap B1 Bit 1	Tap B1 Bit 1	Digital Output
20	Tap B1 Bit 3	Tap B1 Bit 3	Digital Output
21	Tap B1 Bit 5	Tap B1 Bit 5	Digital Output
22	Tap B1 Bit 7	Tap B1 Bit 7	Digital Output
23	Tap B1 Bit 9	Tap B1 Bit 9	Digital Output
24	Tap B1 Bit 11	Tap B1 Bit 11	Digital Output
25	Tap B1 Bit 0	Tap B1 Bit 0	Digital Output
26	Tap B1 Bit 2	Tap B1 Bit 2	Digital Output
27	Tap B1 Bit 4	Tap B1 Bit 4	Digital Output
28	VSS	VSS	Ground

Pin	Signal Name DR-4k-3.5LCC & DR-2x2k-7LCC	Signal Name DR-2k-7LCC	Type
29	Tap B1 Bit 6	Tap B1 Bit 6	Digital Output
30	Tap B1 Bit 8	Tap B1 Bit 8	Digital Output
31	Tap B1 Bit 10	Tap B1 Bit 10	Digital Output
32	Tap B1 Bit 12	Tap B1 Bit 12	Digital Output
33	VSS	VSS	Ground
34	VDDA	VDDA	3.3V Analogue
35	VDD	VDD	3.3V supply
36	VDD	VDD	3.3V supply
37	VDD	VDD	3.3V supply
38	VDDA	VDDA	3.3V Analogue
39	N_Reset	N_Reset	Digital Input
40	VSS	Ground	Ground
41	Tap D1 Bit 12	Not connected	Digital Output
42	Tap D1 Bit 10	Not connected	Digital Output
43	Tap D1 Bit 8	Not connected	Digital Output
44	Tap D1 Bit 6	Not connected	Digital Output
45	VSS	VSS	Ground
46	Tap D1 Bit 4	Not connected	Digital Output
47	Tap D1 Bit 2	Not connected	Digital Output
48	Tap D1 Bit 0	Not connected	Digital Output
49	Tap D1 Bit 11	Not connected	Digital Output
50	Tap D1 Bit 9	Not connected	Digital Output
51	Tap D1 Bit 7	Not connected	Digital Output
52	Tap D1 Bit 5	Not connected	Digital Output
53	Tap D1 Bit 3	Not connected	Digital Output
54	Tap D1 Bit 1	Not connected	Digital Output
55	VSS	Ground	Ground
56	END_ADC_TAP C1/D1	Not connected	Digital Output
57	Pixel_CLK_Tap C1/D1	Not connected	Digital Output
58	Tap C1 Bit 0	Not connected	Digital Output
59	Tap C1 Bit 2	Not connected	Digital Output
60	Tap C1 Bit 4	Not connected	Digital Output
61	Tap C1 Bit 6	Not connected	Digital Output

Pin	Signal Name DR-4k-3.5LCC & DR-2x2k-7LCC	Signal Name DR-2k-7LCC	Type
62	Tap C1 Bit 8	Not connected	Digital Output
63	Tap C1 Bit 10	Not connected	Digital Output
64	Tap C1 Bit 12	Not connected	Digital Output
65	LVAL Tap C1/D1	Not connected	Digital Output
66	VSS	Ground	Ground
67	MISO C1/D1	Not connected	Digital Output
68	Tap C1 Bit 1	Not connected	Digital Output
69	Tap C1 Bit 3	Not connected	Digital Output
70	Tap C1 Bit 5	Not connected	Digital Output
71	Tap C1 Bit 7	Not connected	Digital Output
72	Tap C1 Bit 9	Not connected	Digital Output
73	VSS	Ground	Ground
74	Tap C1 Bit 11	Not connected	Digital Output
75	RESET_CDS	Digital Input	Digital Input
76	N_CS C1/D1	Not connected	Digital Input
77	MOSI	Digital Input	Digital Input
78	Main_CLK	Digital Input	Digital Input
79	Load_Pulse	Digital Input	Digital Input
80	VSS	Ground	Ground
81	VDD	3.3V	3.3V
82	VDD	3.3V	3.3V
83	VDDA	VDDA	3.3V Analogue
84	VDDA	VDDA	3.3V Analogue
85	N_CS A1/B1	Digital Input	Digital Input
86	SAMPLE	Digital Input	Digital Input
87	RST_CVC	Digital Input	Digital Input
88	SCLK	Digital Input	Digital Input
89	MISO A1/B1	Digital Output	Digital Output
90	VSS	Ground	Ground

From LCC version v2.0 there is a separation from chip analogue power to other supplies but without separation on GND pins.

6.2 Connectors for different versions of invar headboard packages

The below table indicates which connectors are present for the different chip versions

Chip version	Present connectors
DR-2k-7LCC	See LCC pin out, no connector
DR-2k-7-invar	CONNECTOR 1 & CONNECTOR 2 (connector 2 is not used)
DR-4k-7	CONNECTOR 1
DR-8k-7	CONNECTOR 1 & CONNECTOR 3
DR-2x2k-7LCC	See LCC pin out, no connector
DR-2x2k-7-invar	CONNECTOR 1 & CONNECTOR 2
DR-2x4k-7	CONNECTOR 1 & CONNECTOR 2
DR-2x8k-7	See LCC pin out, no connector
DR-4k-3.5LCC	CONNECTOR 1 - 4
DR-4k-3.5-invar	CONNECTOR 1 & CONNECTOR 2
DR-8k-3.5	CONNECTOR 1 & CONNECTOR 2
DR-16k-3.5	CONNECTOR 1 - 4

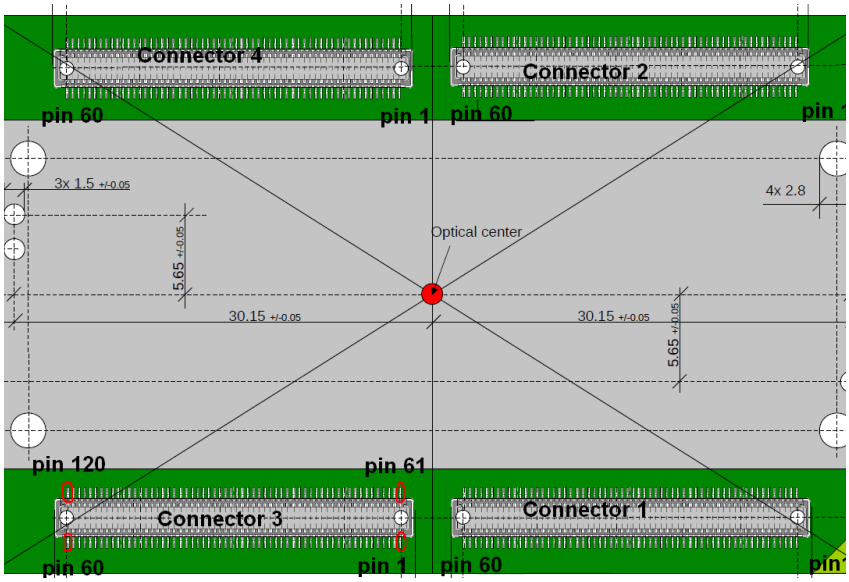


Fig 31: Identification of connector number and pin numbers

6.3 Connector signal assignment for invar head board variations DR-2x2k-7-invar; DR-4k-3.5-invar and DR-2k-7-invar

Note, for DR-2k-7-invar CONNECTOR 2 is present but not required. Only the powers present on the connector are routed to the sensor. CONNECTOR 2 can be left completely unconnected for DR-2k-7-invar.

6.3.1 CONNECTOR 1

Dragster Headboard Connector	Pin Number	Signal Name	Signal Type
CONNECTOR 1	1	VSSESD/IO	GND
CONNECTOR 1	2	LVAL_AB_1	Dig out
CONNECTOR 1	3	BIT_12_TAP_A1	Dig out
CONNECTOR 1	4	BIT_11_TAP_A1	Dig out
CONNECTOR 1	5	BIT_10_TAP_A1	Dig out
CONNECTOR 1	6	BIT_09_TAP_A1	Dig out
CONNECTOR 1	7	BIT_08_TAP_A1	Dig out
CONNECTOR 1	8	BIT_07_TAP_A1	Dig out
CONNECTOR 1	9	BIT_06_TAP_A1	Dig out
CONNECTOR 1	10	BIT_05_TAP_A1	Dig out
CONNECTOR 1	11	BIT_04_TAP_A1	Dig out
CONNECTOR 1	12	BIT_03_TAP_A1	Dig out
CONNECTOR 1	13	BIT_02_TAP_A1	Dig out
CONNECTOR 1	14	BIT_01_TAP_A1	Dig out
CONNECTOR 1	15	BIT_00_TAP_A1	Dig out
CONNECTOR 1	16	VSSESD/IO	GND
CONNECTOR 1	17	BIT_00_TAP_B1	Dig out
CONNECTOR 1	18	BIT_01_TAP_B1	Dig out
CONNECTOR 1	19	BIT_02_TAP_B1	Dig out
CONNECTOR 1	20	BIT_03_TAP_B1	Dig out
CONNECTOR 1	21	BIT_04_TAP_B1	Dig out
CONNECTOR 1	22	BIT_05_TAP_B1	Dig out
CONNECTOR 1	23	BIT_06_TAP_B1	Dig out
CONNECTOR 1	24	BIT_07_TAP_B1	Dig out
CONNECTOR 1	25	BIT_08_TAP_B1	Dig out
CONNECTOR 1	26	BIT_09_TAP_B1	Dig out
CONNECTOR 1	27	BIT_10_TAP_B1	Dig out
CONNECTOR 1	28	BIT_11_TAP_B1	Dig out
CONNECTOR 1	29	BIT_12_TAP_B1	Dig out
CONNECTOR 1	30	MAIN_CLK	Dig in
CONNECTOR 1	31	VSSESD/IO	GND
CONNECTOR 1	32	Not Connected	
CONNECTOR 1	33	Not Connected	
CONNECTOR 1	34	Not Connected	
CONNECTOR 1	35	Not Connected	
CONNECTOR 1	36	Not Connected	
CONNECTOR 1	37	Not Connected	
CONNECTOR 1	38	Not Connected	
CONNECTOR 1	39	Not Connected	
CONNECTOR 1	40	Not Connected	

CONNECTOR 1	41	Not Connected	
CONNECTOR 1	42	Not Connected	
CONNECTOR 1	43	Not Connected	
CONNECTOR 1	44	Not Connected	
CONNECTOR 1	45	Not Connected	
CONNECTOR 1	46	VSSESD/IO	GND
CONNECTOR 1	47	Not Connected	
CONNECTOR 1	48	Not Connected	
CONNECTOR 1	49	Not Connected	
CONNECTOR 1	50	Not Connected	
CONNECTOR 1	51	Not Connected	
CONNECTOR 1	52	Not Connected	
CONNECTOR 1	53	Not Connected	
CONNECTOR 1	54	Not Connected	
CONNECTOR 1	55	Not Connected	
CONNECTOR 1	56	Not Connected	
CONNECTOR 1	57	Not Connected	
CONNECTOR 1	58	Not Connected	
CONNECTOR 1	59	Not Connected	
CONNECTOR 1	60	VSSESD/IO	GND
CONNECTOR 1	61	N_CS_AB_1	Dig in
CONNECTOR 1	62	MISO_AB_1	Dig out
CONNECTOR 1	63	VDDA	VDDA
CONNECTOR 1	64	VDDD	VDDD
CONNECTOR 1	65	VSSA	GND
CONNECTOR 1	66	VSS_BULK	GND
CONNECTOR 1	67	VSSD	GND
CONNECTOR 1	68	LOAD_PULSE_AB_1	Dig in
CONNECTOR 1	69	VDDIO	VDDIO
CONNECTOR 1	70	END_ADC_AB_1	Dig out
CONNECTOR 1	71	VDDA	VDDA
CONNECTOR 1	72	VDD_BULK	VDD_Bulk
CONNECTOR 1	73	VDDD	VDDD
CONNECTOR 1	74	VDDESD	VDDESD
CONNECTOR 1	75	VSSA	GND
CONNECTOR 1	76	VSS_BULK	GND
CONNECTOR 1	77	VSSD	GND
CONNECTOR 1	78	VDDIO	VDDIO
CONNECTOR 1	79	TEST_MUX_AB_1	analogue monitor leave n.c.
CONNECTOR 1	80	VDDA	VDDA
CONNECTOR 1	81	VDDD	VDDD
CONNECTOR 1	82	VSSA	GND
CONNECTOR 1	83	VSS_BULK	GND
CONNECTOR 1	84	VSSD	GND
CONNECTOR 1	85	VSSESD/IO	GND
CONNECTOR 1	86	PIXEL_CLK_AB_1	Dig_out
CONNECTOR 1	87	VCLAMP_AB_1	VDDA
CONNECTOR 1	88	SAMPLE_AB	Dig in
CONNECTOR 1	89	RST_CDS_AB	Dig in
CONNECTOR 1	90	RST_CVC_AB	Dig in
CONNECTOR 1	91	Not Connected	
CONNECTOR 1	92	SCLK_AB_EF	Dig in
CONNECTOR 1	93	MOSI_AB_EF	dig in
CONNECTOR 1	94	Not Connected	

CONNECTOR 1	95	VDDA	VDDA
CONNECTOR 1	96	VDD_BULK	VDD_Bulk
CONNECTOR 1	97	VDDD	VDDD
CONNECTOR 1	98	VDDESD	VDDESD
CONNECTOR 1	99	VSSA	GND
CONNECTOR 1	100	VSS_BULK	GND
CONNECTOR 1	101	VSSD	GND
CONNECTOR 1	102	Not Connected	
CONNECTOR 1	103	VDDIO	VDDIO
CONNECTOR 1	104	Not Connected	
CONNECTOR 1	105	VDDA	VDDA
CONNECTOR 1	106	VDDD	VDDD
CONNECTOR 1	107	VSSA	GND
CONNECTOR 1	108	VSSD	GND
CONNECTOR 1	109	VDDIO	VDDIO
CONNECTOR 1	110	Not Connected	
CONNECTOR 1	111	VDDA	VDDA
CONNECTOR 1	112	VDD_BULK	VDD_Bulk
CONNECTOR 1	113	VDDD	VDDD
CONNECTOR 1	114	VDDESD	VDDESD
CONNECTOR 1	115	VSSA	GND
CONNECTOR 1	116	VSS_BULK	GND
CONNECTOR 1	117	VSSD	GND
CONNECTOR 1	118	N_RESET_AB	Dig in
CONNECTOR 1	119	Not Connected	
CONNECTOR 1	120	Not Connected	

NOTE: SCLK and MOSI are connected between connector 1 and connector 3 in the headboard, resulting names are SCLK_AB_EF and MOSI_AB_EF. User just need to provide to the headboard one pair of this signals to connector 1 or 3 to communicate with the SPI's, taking the advantage that 2 IO lines from the control unit (FPGA or CPLD) are saved. Each SPI can be selected individually by selecting respective negative chip select pin.

6.3.2 CONNECTOR 2

CONNECTOR 2	1	N_CS_CD_1	Dig in
CONNECTOR 2	2	MISO_CD_1	Dig out
CONNECTOR 2	3	VDDA	VDDA
CONNECTOR 2	4	VDDD	VDDD
CONNECTOR 2	5	VSSA	GND
CONNECTOR 2	6	VSS_BULK	GND
CONNECTOR 2	7	VSSD	GND
CONNECTOR 2	8	LOAD_PULSE_CD_1	Dig in
CONNECTOR 2	9	VDDIO	VDDIO
CONNECTOR 2	10	END_ADC_CD_1	Dig out
CONNECTOR 2	11	VDDA	VDDA
CONNECTOR 2	12	VDD_BULK	VDD_Bulk
CONNECTOR 2	13	VDDD	VDDD
CONNECTOR 2	14	VDDESD	VDDESD
CONNECTOR 2	15	VSSA	GND
CONNECTOR 2	16	VSS_BULK	GND
CONNECTOR 2	17	VSSD	GND
CONNECTOR 2	18	VDDIO	VDDIO
CONNECTOR 2	19	TEST_MUX_CD_1	analogue monitor leave n.c.
CONNECTOR 2	20	VDDA	VDDA
CONNECTOR 2	21	VDDD	VDDD
CONNECTOR 2	22	VSSA	GND
CONNECTOR 2	23	VSS_BULK	GND
CONNECTOR 2	24	VSSD	GND
CONNECTOR 2	25	VSSESD/IO	GND
CONNECTOR 2	26	PIXEL_CLK_CD_1	Dig_out
CONNECTOR 2	27	VCLAMP_CD_1	VDDA
CONNECTOR 2	28	SAMPLE_CD	Dig in
CONNECTOR 2	29	RST_CDS_CD	Dig in
CONNECTOR 2	30	RST_CVC_CD	Dig in
CONNECTOR 2	31	Not Connected	
CONNECTOR 2	32	SCLK_CD_GH	Dig in
CONNECTOR 2	33	MOSI_CD_GH	Dig in
CONNECTOR 2	34	Not Connected	
CONNECTOR 2	35	VDDA	VDDA
CONNECTOR 2	36	VDD_BULK	VDD_Bulk
CONNECTOR 2	37	VDDD	VDDD
CONNECTOR 2	38	VDDESD	VDDESD
CONNECTOR 2	39	VSSA	GND
CONNECTOR 2	40	VSS_BULK	GND
CONNECTOR 2	41	VSSD	GND
CONNECTOR 2	42	Not Connected	
CONNECTOR 2	43	VDDIO	VDDIO
CONNECTOR 2	44	Not Connected	
CONNECTOR 2	45	VDDA	VDDA
CONNECTOR 2	46	VDDD	VDDD
CONNECTOR 2	47	VSSA	GND
CONNECTOR 2	48	VSSD	GND
CONNECTOR 2	49	VDDIO	VDDIO
CONNECTOR 2	50	Not Connected	
CONNECTOR 2	51	VDDA	VDDA
CONNECTOR 2	52	VDD_BULK	VDD_Bulk

CONNECTOR 2	53	VDDD	VDDD
CONNECTOR 2	54	VDDESD	VDDESD
CONNECTOR 2	55	VSSA	GND
CONNECTOR 2	56	VSS_BULK	GND
CONNECTOR 2	57	VSSD	GND
CONNECTOR 2	58	N_RESET_CD	Dig in
CONNECTOR 2	59	Not Connected	
CONNECTOR 2	60	Not Connected	
CONNECTOR 2	61	VSSESD/IO	GND
CONNECTOR 2	62	LVAL_CD_1	Dig out
CONNECTOR 2	63	BIT_12_TAP_C1	Dig out
CONNECTOR 2	64	BIT_11_TAP_C1	Dig out
CONNECTOR 2	65	BIT_10_TAP_C1	Dig out
CONNECTOR 2	66	BIT_09_TAP_C1	Dig out
CONNECTOR 2	67	BIT_08_TAP_C1	Dig out
CONNECTOR 2	68	BIT_07_TAP_C1	Dig out
CONNECTOR 2	69	BIT_06_TAP_C1	Dig out
CONNECTOR 2	70	BIT_05_TAP_C1	Dig out
CONNECTOR 2	71	BIT_04_TAP_C1	Dig out
CONNECTOR 2	72	BIT_03_TAP_C1	Dig out
CONNECTOR 2	73	BIT_02_TAP_C1	Dig out
CONNECTOR 2	74	BIT_01_TAP_C1	Dig out
CONNECTOR 2	75	BIT_00_TAP_C1	Dig out
CONNECTOR 2	76	VSSESD/IO	GND
CONNECTOR 2	77	BIT_00_TAP_D1	Dig out
CONNECTOR 2	78	BIT_01_TAP_D1	Dig out
CONNECTOR 2	79	BIT_02_TAP_D1	Dig out
CONNECTOR 2	80	BIT_03_TAP_D1	Dig out
CONNECTOR 2	81	BIT_04_TAP_D1	Dig out
CONNECTOR 2	82	BIT_05_TAP_D1	Dig out
CONNECTOR 2	83	BIT_06_TAP_D1	Dig out
CONNECTOR 2	84	BIT_07_TAP_D1	Dig out
CONNECTOR 2	85	BIT_08_TAP_D1	Dig out
CONNECTOR 2	86	BIT_09_TAP_D1	Dig out
CONNECTOR 2	87	BIT_10_TAP_D1	Dig out
CONNECTOR 2	88	BIT_11_TAP_D1	Dig out
CONNECTOR 2	89	BIT_12_TAP_D1	Dig out
CONNECTOR 2	90	Not Connected	
CONNECTOR 2	91	VSSESD/IO	GND
CONNECTOR 2	92	Not Connected	
CONNECTOR 2	93	Not Connected	
CONNECTOR 2	94	Not Connected	
CONNECTOR 2	95	Not Connected	
CONNECTOR 2	96	Not Connected	
CONNECTOR 2	97	Not Connected	
CONNECTOR 2	98	Not Connected	
CONNECTOR 2	99	Not Connected	
CONNECTOR 2	100	Not Connected	
CONNECTOR 2	101	Not Connected	
CONNECTOR 2	102	Not Connected	
CONNECTOR 2	103	Not Connected	
CONNECTOR 2	104	Not Connected	
CONNECTOR 2	105	Not Connected	
CONNECTOR 2	106	VSSESD/IO	GND

CONNECTOR 2	107	Not Connected	
CONNECTOR 2	108	Not Connected	
CONNECTOR 2	109	Not Connected	
CONNECTOR 2	110	Not Connected	
CONNECTOR 2	111	Not Connected	
CONNECTOR 2	112	Not Connected	
CONNECTOR 2	113	Not Connected	
CONNECTOR 2	114	Not Connected	
CONNECTOR 2	115	Not Connected	
CONNECTOR 2	116	Not Connected	
CONNECTOR 2	117	Not Connected	
CONNECTOR 2	118	Not Connected	
CONNECTOR 2	119	Not Connected	
CONNECTOR 2	120	VSSESD/IO	GND

NOTE: SCLK and MOSI are connected between connector 2 and connector 4 in the headboard, resulting names are SCLK_CD_GH and MOSI_CD_GH. The user just need to provide to the headboard one pair of this signals to connector 2 or 4 to communicate with the SPI's, taking the advantage that 2 IO lines from the control unit (FPGA or CPLD) are saved. Each SPI can be selected individually by selecting respective negative chip select pin.

6.4 Connector signal assignment for invar head board variations DR-4k-7; DR-8k-7; DR-8k-3.5; DR-16k-3.5, DR-2x4k-7; DR-2x8k-7

The signal assignment for all invar type headboards is identical, though for smaller chip versions some connectors may not be present. check section 6.2 for a listing of present connectors on the different chip variations. The pin numbers are cyclic, when looking on the connector form the connector side right to left.

6.4.1 CONNECTOR 1

Dragster Headboard Connector	Pin Number	Signal Name	Signal Type
CONNECTOR 1	1	VSSESD/IO	GND
CONNECTOR 1	2	LVAL_AB_1	Dig out
CONNECTOR 1	3	BIT_12_TAP_A1	Dig out
CONNECTOR 1	4	BIT_11_TAP_A1	Dig out
CONNECTOR 1	5	BIT_10_TAP_A1	Dig out
CONNECTOR 1	6	BIT_09_TAP_A1	Dig out
CONNECTOR 1	7	BIT_08_TAP_A1	Dig out
CONNECTOR 1	8	BIT_07_TAP_A1	Dig out
CONNECTOR 1	9	BIT_06_TAP_A1	Dig out
CONNECTOR 1	10	BIT_05_TAP_A1	Dig out
CONNECTOR 1	11	BIT_04_TAP_A1	Dig out
CONNECTOR 1	12	BIT_03_TAP_A1	Dig out
CONNECTOR 1	13	BIT_02_TAP_A1	Dig out
CONNECTOR 1	14	BIT_01_TAP_A1	Dig out
CONNECTOR 1	15	BIT_00_TAP_A1	Dig out
CONNECTOR 1	16	VSSESD/IO	GND
CONNECTOR 1	17	BIT_00_TAP_B1	Dig out
CONNECTOR 1	18	BIT_01_TAP_B1	Dig out
CONNECTOR 1	19	BIT_02_TAP_B1	Dig out
CONNECTOR 1	20	BIT_03_TAP_B1	Dig out
CONNECTOR 1	21	BIT_04_TAP_B1	Dig out
CONNECTOR 1	22	BIT_05_TAP_B1	Dig out
CONNECTOR 1	23	BIT_06_TAP_B1	Dig out
CONNECTOR 1	24	BIT_07_TAP_B1	Dig out
CONNECTOR 1	25	BIT_08_TAP_B1	Dig out
CONNECTOR 1	26	BIT_09_TAP_B1	Dig out
CONNECTOR 1	27	BIT_10_TAP_B1	Dig out
CONNECTOR 1	28	BIT_11_TAP_B1	Dig out
CONNECTOR 1	29	BIT_12_TAP_B1	Dig out
CONNECTOR 1	30	MAIN_CLK	Dig in
CONNECTOR 1	31	VSSESD/IO	GND
CONNECTOR 1	32	LVAL_AB_2	Dig out
CONNECTOR 1	33	BIT_12_TAP_A2	Dig out
CONNECTOR 1	34	BIT_11_TAP_A2	Dig out
CONNECTOR 1	35	BIT_10_TAP_A2	Dig out
CONNECTOR 1	36	BIT_09_TAP_A2	Dig out
CONNECTOR 1	37	BIT_08_TAP_A2	Dig out
CONNECTOR 1	38	BIT_07_TAP_A2	Dig out
CONNECTOR 1	39	BIT_06_TAP_A2	Dig out

CONNECTOR 1	40	BIT_05_TAP_A2	Dig out
CONNECTOR 1	41	BIT_04_TAP_A2	Dig out
CONNECTOR 1	42	BIT_03_TAP_A2	Dig out
CONNECTOR 1	43	BIT_02_TAP_A2	Dig out
CONNECTOR 1	44	BIT_01_TAP_A2	Dig out
CONNECTOR 1	45	BIT_00_TAP_A2	Dig out
CONNECTOR 1	46	VSSESD/IO	GND
CONNECTOR 1	47	BIT_00_TAP_B2	Dig out
CONNECTOR 1	48	BIT_01_TAP_B2	Dig out
CONNECTOR 1	49	BIT_02_TAP_B2	Dig out
CONNECTOR 1	50	BIT_03_TAP_B2	Dig out
CONNECTOR 1	51	BIT_04_TAP_B2	Dig out
CONNECTOR 1	52	BIT_05_TAP_B2	Dig out
CONNECTOR 1	53	BIT_06_TAP_B2	Dig out
CONNECTOR 1	54	BIT_07_TAP_B2	Dig out
CONNECTOR 1	55	BIT_08_TAP_B2	Dig out
CONNECTOR 1	56	BIT_09_TAP_B2	Dig out
CONNECTOR 1	57	BIT_10_TAP_B2	Dig out
CONNECTOR 1	58	BIT_11_TAP_B2	Dig out
CONNECTOR 1	59	BIT_12_TAP_B2	Dig out
CONNECTOR 1	60	VSSESD/IO	GND
CONNECTOR 1	61	N_CS_AB_1	Dig in
CONNECTOR 1	62	MISO_AB_1	Dig out
CONNECTOR 1	63	VDDA	VDDA
CONNECTOR 1	64	VDDD	VDDD
CONNECTOR 1	65	VSSA	GND
CONNECTOR 1	66	VSS_BULK	GND
CONNECTOR 1	67	VSSD	GND
CONNECTOR 1	68	LOAD_PULSE_AB_1	Dig in
CONNECTOR 1	69	VDDIO	VDDIO
CONNECTOR 1	70	END_ADC_AB_1	Dig out
CONNECTOR 1	71	VDDA	VDDA
CONNECTOR 1	72	VDD_BULK	VDD_Bulk
CONNECTOR 1	73	VDDD	VDDD
CONNECTOR 1	74	VDDESD	VDDESD
CONNECTOR 1	75	VSSA	GND
CONNECTOR 1	76	VSS_BULK	GND
CONNECTOR 1	77	VSSD	GND
CONNECTOR 1	78	VDDIO	VDDIO
CONNECTOR 1	79	TEST_MUX_AB_1	analogue monitor leave n.c.
CONNECTOR 1	80	VDDA	VDDA
CONNECTOR 1	81	VDDD	VDDD
CONNECTOR 1	82	VSSA	GND
CONNECTOR 1	83	VSS_BULK	GND
CONNECTOR 1	84	VSSD	GND
CONNECTOR 1	85	VSSESD/IO	GND
CONNECTOR 1	86	PIXEL_CLK_AB_1	Dig_out
CONNECTOR 1	87	VCLAMP_AB_1	VDDA
CONNECTOR 1	88	SAMPLE_AB	Dig in
CONNECTOR 1	89	RST_CDS_AB	Dig in
CONNECTOR 1	90	RST_CVC_AB	Dig in
CONNECTOR 1	91	N_CS_AB_2	Dig in
CONNECTOR 1	92	SCLK_AB_EF	Dig in
CONNECTOR 1	93	MOSI_AB_EF	dig in

CONNECTOR 1	94	MISO_AB_2	Dig out
CONNECTOR 1	95	VDDA	VDDA
CONNECTOR 1	96	VDD_BULK	VDD_Bulk
CONNECTOR 1	97	VDDD	VDDD
CONNECTOR 1	98	VDDESD	VDDESD
CONNECTOR 1	99	VSSA	GND
CONNECTOR 1	100	VSS_BULK	GND
CONNECTOR 1	101	VSSD	GND
CONNECTOR 1	102	LOAD_PULSE_AB_2	Dig in
CONNECTOR 1	103	VDDIO	VDDIO
CONNECTOR 1	104	END_ADC_AB_2	Dig out
CONNECTOR 1	105	VDDA	VDDA
CONNECTOR 1	106	VDDD	VDDD
CONNECTOR 1	107	VSSA	GND
CONNECTOR 1	108	VSSD	GND
CONNECTOR 1	109	VDDIO	VDDIO
CONNECTOR 1	110	TEST_MUX_AB_2	analogue monitor leave n.c.
CONNECTOR 1	111	VDDA	VDDA
CONNECTOR 1	112	VDD_BULK	VDD_Bulk
CONNECTOR 1	113	VDDD	VDDD
CONNECTOR 1	114	VDDESD	VDDESD
CONNECTOR 1	115	VSSA	GND
CONNECTOR 1	116	VSS_BULK	GND
CONNECTOR 1	117	VSSD	GND
CONNECTOR 1	118	N_RESET_AB	Dig in
CONNECTOR 1	119	PIXEL_CLOCK_AB_2	Dig out
CONNECTOR 1	120	VCLAMP_AB_2	VDDA

NOTE: SCLK and MOSI are connected between connector 1 and connector 3 in the headboard, resulting names are SCLK_AB_EF and MOSI_AB_EF. User just need to provide to the headboard one pair of this signals to connector 1 or 3 to communicate with the SPI's, taking the advantage that 2 IO lines from the control unit (FPGA or CPLD) are saved. Each SPI can be selected individually by selecting respective negative chip select pin.

6.4.2 CONNECTOR 2

CONNECTOR 2	1	N_CS_CD_1	Dig in
CONNECTOR 2	2	MISO_CD_1	Dig out
CONNECTOR 2	3	VDDA	VDDA
CONNECTOR 2	4	VDDD	VDDD
CONNECTOR 2	5	VSSA	GND
CONNECTOR 2	6	VSS_BULK	GND
CONNECTOR 2	7	VSSD	GND
CONNECTOR 2	8	LOAD_PULSE_CD_1	Dig in
CONNECTOR 2	9	VDDIO	VDDIO
CONNECTOR 2	10	END_ADC_CD_1	Dig out
CONNECTOR 2	11	VDDA	VDDA
CONNECTOR 2	12	VDD_BULK	VDD_Bulk
CONNECTOR 2	13	VDDD	VDDD
CONNECTOR 2	14	VDDESD	VDDESD
CONNECTOR 2	15	VSSA	GND
CONNECTOR 2	16	VSS_BULK	GND
CONNECTOR 2	17	VSSD	GND
CONNECTOR 2	18	VDDIO	VDDIO
CONNECTOR 2	19	TEST_MUX_CD_1	analogue monitor leave n.c.
CONNECTOR 2	20	VDDA	VDDA
CONNECTOR 2	21	VDDD	VDDD
CONNECTOR 2	22	VSSA	GND
CONNECTOR 2	23	VSS_BULK	GND
CONNECTOR 2	24	VSSD	GND
CONNECTOR 2	25	VSSESD/IO	GND
CONNECTOR 2	26	PIXEL_CLK_CD_1	Dig_out
CONNECTOR 2	27	VCLAMP_CD_1	VDDA
CONNECTOR 2	28	SAMPLE_CD	Dig in
CONNECTOR 2	29	RST_CDS_CD	Dig in
CONNECTOR 2	30	RST_CVC_CD	Dig in
CONNECTOR 2	31	N_CS_CD_2	Dig in
CONNECTOR 2	32	SCLK_CD_GH	Dig in
CONNECTOR 2	33	MOSI_CD_GH	Dig in
CONNECTOR 2	34	MISO_CD_2	Dig out
CONNECTOR 2	35	VDDA	VDDA
CONNECTOR 2	36	VDD_BULK	VDD_Bulk
CONNECTOR 2	37	VDDD	VDDD
CONNECTOR 2	38	VDDESD	VDDESD
CONNECTOR 2	39	VSSA	GND
CONNECTOR 2	40	VSS_BULK	GND
CONNECTOR 2	41	VSSD	GND
CONNECTOR 2	42	LOAD_PULSE_CD_2	Dig in
CONNECTOR 2	43	VDDIO	VDDIO
CONNECTOR 2	44	END_ADC_CD_2	Dig out
CONNECTOR 2	45	VDDA	VDDA
CONNECTOR 2	46	VDDD	VDDD
CONNECTOR 2	47	VSSA	GND
CONNECTOR 2	48	VSSD	GND
CONNECTOR 2	49	VDDIO	VDDIO
CONNECTOR 2	50	TEST_MUX_CD_2	analogue monitor leave n.c.
CONNECTOR 2	51	VDDA	VDDA
CONNECTOR 2	52	VDD_BULK	VDD_Bulk

CONNECTOR 2	53	VDDD	VDDD
CONNECTOR 2	54	VDDESD	VDDESD
CONNECTOR 2	55	VSSA	GND
CONNECTOR 2	56	VSS_BULK	GND
CONNECTOR 2	57	VSSD	GND
CONNECTOR 2	58	N_RESET_CD	Dig in
CONNECTOR 2	59	PIXEL_CLK_CD_2	Dig_out
CONNECTOR 2	60	VCLAMP_CD_2	VDDA
CONNECTOR 2	61	VSSESD/IO	GND
CONNECTOR 2	62	LVAL_CD_1	Dig out
CONNECTOR 2	63	BIT_12_TAP_C1	Dig out
CONNECTOR 2	64	BIT_11_TAP_C1	Dig out
CONNECTOR 2	65	BIT_10_TAP_C1	Dig out
CONNECTOR 2	66	BIT_09_TAP_C1	Dig out
CONNECTOR 2	67	BIT_08_TAP_C1	Dig out
CONNECTOR 2	68	BIT_07_TAP_C1	Dig out
CONNECTOR 2	69	BIT_06_TAP_C1	Dig out
CONNECTOR 2	70	BIT_05_TAP_C1	Dig out
CONNECTOR 2	71	BIT_04_TAP_C1	Dig out
CONNECTOR 2	72	BIT_03_TAP_C1	Dig out
CONNECTOR 2	73	BIT_02_TAP_C1	Dig out
CONNECTOR 2	74	BIT_01_TAP_C1	Dig out
CONNECTOR 2	75	BIT_00_TAP_C1	Dig out
CONNECTOR 2	76	VSSESD/IO	GND
CONNECTOR 2	77	BIT_00_TAP_D1	Dig out
CONNECTOR 2	78	BIT_01_TAP_D1	Dig out
CONNECTOR 2	79	BIT_02_TAP_D1	Dig out
CONNECTOR 2	80	BIT_03_TAP_D1	Dig out
CONNECTOR 2	81	BIT_04_TAP_D1	Dig out
CONNECTOR 2	82	BIT_05_TAP_D1	Dig out
CONNECTOR 2	83	BIT_06_TAP_D1	Dig out
CONNECTOR 2	84	BIT_07_TAP_D1	Dig out
CONNECTOR 2	85	BIT_08_TAP_D1	Dig out
CONNECTOR 2	86	BIT_09_TAP_D1	Dig out
CONNECTOR 2	87	BIT_10_TAP_D1	Dig out
CONNECTOR 2	88	BIT_11_TAP_D1	Dig out
CONNECTOR 2	89	BIT_12_TAP_D1	Dig out
CONNECTOR 2	90	NC	not connected
CONNECTOR 2	91	VSSESD/IO	GND
CONNECTOR 2	92	LVAL_CD_2	Dig out
CONNECTOR 2	93	BIT_12_TAP_C2	Dig out
CONNECTOR 2	94	BIT_11_TAP_C2	Dig out
CONNECTOR 2	95	BIT_10_TAP_C2	Dig out
CONNECTOR 2	96	BIT_09_TAP_C2	Dig out
CONNECTOR 2	97	BIT_08_TAP_C2	Dig out
CONNECTOR 2	98	BIT_07_TAP_C2	Dig out
CONNECTOR 2	99	BIT_06_TAP_C2	Dig out
CONNECTOR 2	100	BIT_05_TAP_C2	Dig out
CONNECTOR 2	101	BIT_04_TAP_C2	Dig out
CONNECTOR 2	102	BIT_03_TAP_C2	Dig out
CONNECTOR 2	103	BIT_02_TAP_C2	Dig out
CONNECTOR 2	104	BIT_01_TAP_C2	Dig out
CONNECTOR 2	105	BIT_00_TAP_C2	Dig out
CONNECTOR 2	106	VSSESD/IO	GND

CONNECTOR 2	107	BIT_00_TAP_D2	Dig out
CONNECTOR 2	108	BIT_01_TAP_D2	Dig out
CONNECTOR 2	109	BIT_02_TAP_D2	Dig out
CONNECTOR 2	110	BIT_03_TAP_D2	Dig out
CONNECTOR 2	111	BIT_04_TAP_D2	Dig out
CONNECTOR 2	112	BIT_05_TAP_D2	Dig out
CONNECTOR 2	113	BIT_06_TAP_D2	Dig out
CONNECTOR 2	114	BIT_07_TAP_D2	Dig out
CONNECTOR 2	115	BIT_08_TAP_D2	Dig out
CONNECTOR 2	116	BIT_09_TAP_D2	Dig out
CONNECTOR 2	117	BIT_10_TAP_D2	Dig out
CONNECTOR 2	118	BIT_11_TAP_D2	Dig out
CONNECTOR 2	119	BIT_12_TAP_D2	Dig out
CONNECTOR 2	120	VSSESD/IO	GND

NOTE: SCLK and MOSI are connected between connector 2 and connector 4 in the headboard, resulting names are SCLK_CD_GH and MOSI_CD_GH. The user just need to provide to the headboard one pair of this signals to connector 2 or 4 to communicate with the SPI's, taking the advantage that 2 IO lines from the control unit (FPGA or CPLD) are saved. Each SPI can be selected individually by selecting respective negative chip select pin.

6.4.3 CONNECTOR 3

(identical to connector 1 exception of mclk)

Dragster Headboard Connector	Pin Number	Signal Name	Signal Type
CONNECTOR 3	1	VSSESD/IO	GND
CONNECTOR 3	2	LVAL_EF_1	Dig out
CONNECTOR 3	3	BIT_12_TAP_E1	Dig out
CONNECTOR 3	4	BIT_11_TAP_E1	Dig out
CONNECTOR 3	5	BIT_10_TAP_E1	Dig out
CONNECTOR 3	6	BIT_09_TAP_E1	Dig out
CONNECTOR 3	7	BIT_08_TAP_E1	Dig out
CONNECTOR 3	8	BIT_07_TAP_E1	Dig out
CONNECTOR 3	9	BIT_06_TAP_E1	Dig out
CONNECTOR 3	10	BIT_05_TAP_E1	Dig out
CONNECTOR 3	11	BIT_04_TAP_E1	Dig out
CONNECTOR 3	12	BIT_03_TAP_E1	Dig out
CONNECTOR 3	13	BIT_02_TAP_E1	Dig out
CONNECTOR 3	14	BIT_01_TAP_E1	Dig out
CONNECTOR 3	15	BIT_00_TAP_E1	Dig out
CONNECTOR 3	16	VSSESD/IO	GND
CONNECTOR 3	17	BIT_00_TAP_F1	Dig out
CONNECTOR 3	18	BIT_01_TAP_F1	Dig out
CONNECTOR 3	19	BIT_02_TAP_F1	Dig out
CONNECTOR 3	20	BIT_03_TAP_F1	Dig out
CONNECTOR 3	21	BIT_04_TAP_F1	Dig out
CONNECTOR 3	22	BIT_05_TAP_F1	Dig out
CONNECTOR 3	23	BIT_06_TAP_F1	Dig out
CONNECTOR 3	24	BIT_07_TAP_F1	Dig out
CONNECTOR 3	25	BIT_08_TAP_F1	Dig out
CONNECTOR 3	26	BIT_09_TAP_F1	Dig out
CONNECTOR 3	27	BIT_10_TAP_F1	Dig out
CONNECTOR 3	28	BIT_11_TAP_F1	Dig out
CONNECTOR 3	29	BIT_12_TAP_F1	Dig out
CONNECTOR 3	30	MAIN_CLK	Dig in
CONNECTOR 3	31	VSSESD/IO	GND
CONNECTOR 3	32	LVAL_EF_2	Dig out
CONNECTOR 3	33	BIT_12_TAP_E2	Dig out
CONNECTOR 3	34	BIT_11_TAP_E2	Dig out
CONNECTOR 3	35	BIT_10_TAP_E2	Dig out
CONNECTOR 3	36	BIT_09_TAP_E2	Dig out
CONNECTOR 3	37	BIT_08_TAP_E2	Dig out
CONNECTOR 3	38	BIT_07_TAP_E2	Dig out
CONNECTOR 3	39	BIT_06_TAP_E2	Dig out
CONNECTOR 3	40	BIT_05_TAP_E2	Dig out
CONNECTOR 3	41	BIT_04_TAP_E2	Dig out
CONNECTOR 3	42	BIT_03_TAP_E2	Dig out
CONNECTOR 3	43	BIT_02_TAP_E2	Dig out
CONNECTOR 3	44	BIT_01_TAP_E2	Dig out
CONNECTOR 3	45	BIT_00_TAP_E2	Dig out
CONNECTOR 3	46	VSSESD/IO	GND
CONNECTOR 3	47	BIT_00_TAP_F2	Dig out

CONNECTOR 3	48	BIT_01_TAP_F2	Dig out
CONNECTOR 3	49	BIT_02_TAP_F2	Dig out
CONNECTOR 3	50	BIT_03_TAP_F2	Dig out
CONNECTOR 3	51	BIT_04_TAP_F2	Dig out
CONNECTOR 3	52	BIT_05_TAP_F2	Dig out
CONNECTOR 3	53	BIT_06_TAP_F2	Dig out
CONNECTOR 3	54	BIT_07_TAP_F2	Dig out
CONNECTOR 3	55	BIT_08_TAP_F2	Dig out
CONNECTOR 3	56	BIT_09_TAP_F2	Dig out
CONNECTOR 3	57	BIT_10_TAP_F2	Dig out
CONNECTOR 3	58	BIT_11_TAP_F2	Dig out
CONNECTOR 3	59	BIT_12_TAP_F2	Dig out
CONNECTOR 3	60	VSSESD/IO	GND
CONNECTOR 3	61	N_CS_EF_1	Dig in
CONNECTOR 3	62	MISO_EF_1	Dig out
CONNECTOR 3	63	VDDA	VDDA
CONNECTOR 3	64	VDDD	VDDD
CONNECTOR 3	65	VSSA	GND
CONNECTOR 3	66	VSS_BULK	GND
CONNECTOR 3	67	VSSD	GND
CONNECTOR 3	68	LOAD_PULSE_EF_1	Dig in
CONNECTOR 3	69	VDDIO	VDDIO
CONNECTOR 3	70	END_ADC_EF_1	Dig out
CONNECTOR 3	71	VDDA	VDDA
CONNECTOR 3	72	VDD_BULK	VDD_Bulk
CONNECTOR 3	73	VDDD	VDDD
CONNECTOR 3	74	VDDESD	VDDESD
CONNECTOR 3	75	VSSA	GND
CONNECTOR 3	76	VSS_BULK	GND
CONNECTOR 3	77	VSSD	GND
CONNECTOR 3	78	VDDIO	VDDIO
CONNECTOR 3	79	TEST_MUX_EF_1	analogue monitor leave n.c.
CONNECTOR 3	80	VDDA	VDDA
CONNECTOR 3	81	VDDD	VDDD
CONNECTOR 3	82	VSSA	GND
CONNECTOR 3	83	VSS_BULK	GND
CONNECTOR 3	84	VSSD	GND
CONNECTOR 3	85	VSSESD/IO	GND
CONNECTOR 3	86	PIXEL_CLK_EF_1	Dig_out
CONNECTOR 3	87	VCLAMP_EF_1	VDDA
CONNECTOR 3	88	SAMPLE_EF	Dig in
CONNECTOR 3	89	RST_CDS_EF	Dig in
CONNECTOR 3	90	RST_CVC_EF	Dig in
CONNECTOR 3	91	N_CS_EF_2	Dig in
CONNECTOR 3	92	SCLK_AB_EF	Dig in
CONNECTOR 3	93	MOSI_AB_EF	dig in
CONNECTOR 3	94	MISO_EF_2	Dig out
CONNECTOR 3	95	VDDA	VDDA
CONNECTOR 3	96	VDD_BULK	VDD_Bulk
CONNECTOR 3	97	VDDD	VDDD
CONNECTOR 3	98	VDDESD	VDDESD
CONNECTOR 3	99	VSSA	GND
CONNECTOR 3	100	VSS_BULK	GND
CONNECTOR 3	101	VSSD	GND

CONNECTOR 3	102	LOAD_PULSE_EF_2	Dig in
CONNECTOR 3	103	VDDIO	VDDIO
CONNECTOR 3	104	END_ADC_EF_2	Dig out
CONNECTOR 3	105	VDDA	VDDA
CONNECTOR 3	106	VDDD	VDDD
CONNECTOR 3	107	VSSA	GND
CONNECTOR 3	108	VSSD	GND
CONNECTOR 3	109	VDDIO	VDDIO
CONNECTOR 3	110	TEST_MUX_EF_2	analogue monitor leave n.c.
CONNECTOR 3	111	VDDA	VDDA
CONNECTOR 3	112	VDD_BULK	VDD_Bulk
CONNECTOR 3	113	VDDD	VDDD
CONNECTOR 3	114	VDDESD	VDDESD
CONNECTOR 3	115	VSSA	GND
CONNECTOR 3	116	VSS_BULK	GND
CONNECTOR 3	117	VSSD	GND
CONNECTOR 3	118	N_RESET_EF	Dig in
CONNECTOR 3	119	PIXEL_CLOCK_EF_2	Dig out
CONNECTOR 3	120	VCLAMP_EF_2	VDDA

6.4.4 CONNECTOR 4

(identical to Connector 2 exception mclk)

CONNECTOR 4	1	N_CS_GH_1	Dig in
CONNECTOR 4	2	MISO_GH_1	Dig out
CONNECTOR 4	3	VDDA	VDDA
CONNECTOR 4	4	VDDD	VDDD
CONNECTOR 4	5	VSSA	GND
CONNECTOR 4	6	VSS_BULK	GND
CONNECTOR 4	7	VSSD	GND
CONNECTOR 4	8	LOAD_PULSE_GH_1	Dig in
CONNECTOR 4	9	VDDIO	VDDIO
CONNECTOR 4	10	END_ADC_GH_1	Dig out
CONNECTOR 4	11	VDDA	VDDA
CONNECTOR 4	12	VDD_BULK	VDD_Bulk
CONNECTOR 4	13	VDDD	VDDD
CONNECTOR 4	14	VDDESD	VDDESD
CONNECTOR 4	15	VSSA	GND
CONNECTOR 4	16	VSS_BULK	GND
CONNECTOR 4	17	VSSD	GND
CONNECTOR 4	18	VDDIO	VDDIO
CONNECTOR 4	19	TEST_MUX_GH_1	analogue monitor leave n.c.
CONNECTOR 4	20	VDDA	VDDA
CONNECTOR 4	21	VDDD	VDDD
CONNECTOR 4	22	VSSA	GND
CONNECTOR 4	23	VSS_BULK	GND
CONNECTOR 4	24	VSSD	GND
CONNECTOR 4	25	VSSESD/IO	GND
CONNECTOR 4	26	PIXEL_CLK_GH_1	Dig_out
CONNECTOR 4	27	VCLAMP_GH_1	VDDA
CONNECTOR 4	28	SAMPLE_GH	Dig in
CONNECTOR 4	29	RST_CDS_GH	Dig in
CONNECTOR 4	30	RST_CVC_GH	Dig in
CONNECTOR 4	31	N_CS_GH_2	Dig in
CONNECTOR 4	32	SCLK_CD_GH	Dig in
CONNECTOR 4	33	MOSI_CD_GH	Dig in
CONNECTOR 4	34	MISO_GH_2	Dig out
CONNECTOR 4	35	VDDA	VDDA
CONNECTOR 4	36	VDD_BULK	VDD_Bulk
CONNECTOR 4	37	VDDD	VDDD
CONNECTOR 4	38	VDDESD	VDDESD
CONNECTOR 4	39	VSSA	GND
CONNECTOR 4	40	VSS_BULK	GND
CONNECTOR 4	41	VSSD	GND
CONNECTOR 4	42	LOAD_PULSE_GH_2	Dig in
CONNECTOR 4	43	VDDIO	VDDIO
CONNECTOR 4	44	END_ADC_GH_2	Dig out
CONNECTOR 4	45	VDDA	VDDA
CONNECTOR 4	46	VDDD	VDDD
CONNECTOR 4	47	VSSA	GND
CONNECTOR 4	48	VSSD	GND
CONNECTOR 4	49	VDDIO	VDDIO
CONNECTOR 4	50	TEST_MUX_GH_2	analogue monitor leave n.c.

CONNECTOR 4	51	VDDA	VDDA
CONNECTOR 4	52	VDD_BULK	VDD_Bulk
CONNECTOR 4	53	VDDD	VDDD
CONNECTOR 4	54	VDDESD	VDDESD
CONNECTOR 4	55	VSSA	GND
CONNECTOR 4	56	VSS_BULK	GND
CONNECTOR 4	57	VSSD	GND
CONNECTOR 4	58	N_RESET_GH	Dig in
CONNECTOR 4	59	PIXEL_CLK_GH_2	Dig_out
CONNECTOR 4	60	VCLAMP_GH_2	VDDA
CONNECTOR 4	61	VSSESD/IO	GND
CONNECTOR 4	62	LVAL_GH_1	Dig out
CONNECTOR 4	63	BIT_12_TAP_G1	Dig out
CONNECTOR 4	64	BIT_11_TAP_G1	Dig out
CONNECTOR 4	65	BIT_10_TAP_G1	Dig out
CONNECTOR 4	66	BIT_09_TAP_G1	Dig out
CONNECTOR 4	67	BIT_08_TAP_G1	Dig out
CONNECTOR 4	68	BIT_07_TAP_G1	Dig out
CONNECTOR 4	69	BIT_06_TAP_G1	Dig out
CONNECTOR 4	70	BIT_05_TAP_G1	Dig out
CONNECTOR 4	71	BIT_04_TAP_G1	Dig out
CONNECTOR 4	72	BIT_03_TAP_G1	Dig out
CONNECTOR 4	73	BIT_02_TAP_G1	Dig out
CONNECTOR 4	74	BIT_01_TAP_G1	Dig out
CONNECTOR 4	75	BIT_00_TAP_G1	Dig out
CONNECTOR 4	76	VSSESD/IO	GND
CONNECTOR 4	77	BIT_00_TAP_H1	Dig out
CONNECTOR 4	78	BIT_01_TAP_H1	Dig out
CONNECTOR 4	79	BIT_02_TAP_H1	Dig out
CONNECTOR 4	80	BIT_03_TAP_H1	Dig out
CONNECTOR 4	81	BIT_04_TAP_H1	Dig out
CONNECTOR 4	82	BIT_05_TAP_H1	Dig out
CONNECTOR 4	83	BIT_06_TAP_H1	Dig out
CONNECTOR 4	84	BIT_07_TAP_H1	Dig out
CONNECTOR 4	85	BIT_08_TAP_H1	Dig out
CONNECTOR 4	86	BIT_09_TAP_H1	Dig out
CONNECTOR 4	87	BIT_10_TAP_H1	Dig out
CONNECTOR 4	88	BIT_11_TAP_H1	Dig out
CONNECTOR 4	89	BIT_12_TAP_H1	Dig out
CONNECTOR 4	90	NC	not connected
CONNECTOR 4	91	VSSESD/IO	GND
CONNECTOR 4	92	LVAL_GH_2	Dig out
CONNECTOR 4	93	BIT_12_TAP_G2	Dig out
CONNECTOR 4	94	BIT_11_TAP_G2	Dig out
CONNECTOR 4	95	BIT_10_TAP_G2	Dig out
CONNECTOR 4	96	BIT_09_TAP_G2	Dig out
CONNECTOR 4	97	BIT_08_TAP_G2	Dig out
CONNECTOR 4	98	BIT_07_TAP_G2	Dig out
CONNECTOR 4	99	BIT_06_TAP_G2	Dig out
CONNECTOR 4	100	BIT_05_TAP_G2	Dig out
CONNECTOR 4	101	BIT_04_TAP_G2	Dig out
CONNECTOR 4	102	BIT_03_TAP_G2	Dig out
CONNECTOR 4	103	BIT_02_TAP_G2	Dig out
CONNECTOR 4	104	BIT_01_TAP_G2	Dig out

CONNECTOR 4	105	BIT_00_TAP_G2	Dig out
CONNECTOR 4	106	VSSESD/IO	GND
CONNECTOR 4	107	BIT_00_TAP_H2	Dig out
CONNECTOR 4	108	BIT_01_TAP_H2	Dig out
CONNECTOR 4	109	BIT_02_TAP_H2	Dig out
CONNECTOR 4	110	BIT_03_TAP_H2	Dig out
CONNECTOR 4	111	BIT_04_TAP_H2	Dig out
CONNECTOR 4	112	BIT_05_TAP_H2	Dig out
CONNECTOR 4	113	BIT_06_TAP_H2	Dig out
CONNECTOR 4	114	BIT_07_TAP_H2	Dig out
CONNECTOR 4	115	BIT_08_TAP_H2	Dig out
CONNECTOR 4	116	BIT_09_TAP_H2	Dig out
CONNECTOR 4	117	BIT_10_TAP_H2	Dig out
CONNECTOR 4	118	BIT_11_TAP_H2	Dig out
CONNECTOR 4	119	BIT_12_TAP_H2	Dig out
CONNECTOR 4	120	VSSESD/IO	GND

All 4 connectors are of type:
Molex 120 Pin (0,4mm Pitch) Plug 55339-1208

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