TH7813A/TH7814A
50 MHz 1024/2048 Linear CCD

Datasheet

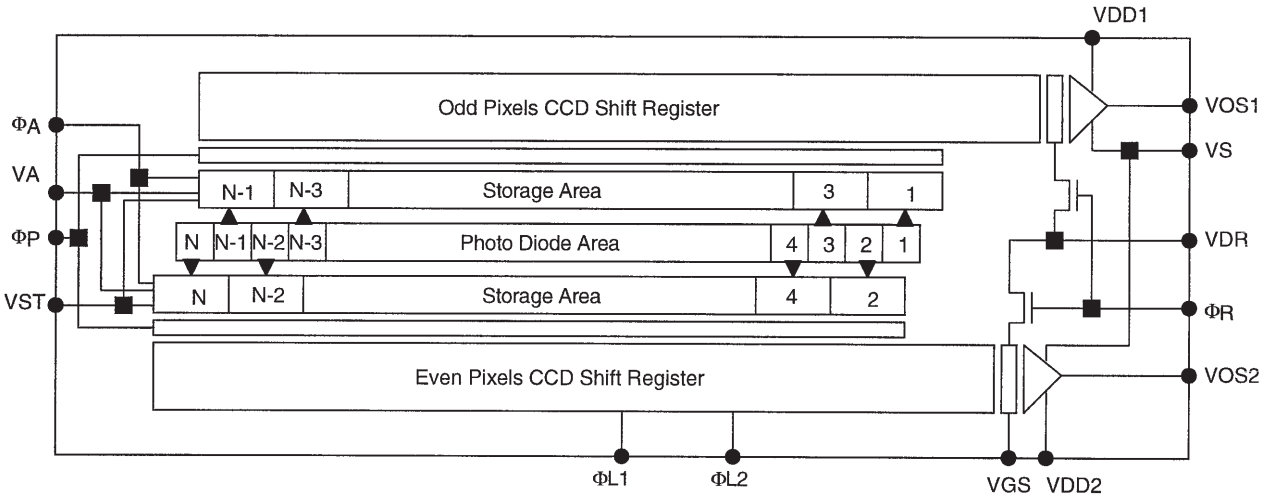
1. Features

- **Data Rate up to 50 MHz (Two Outputs at 25 MHz each)**
- **Pixel Size: 10 µm x 10 µm (10 µm Pitch)**
- **250 to 1100 nm Spectral Range**
- **High Sensitivity and Lag-free Photodiodes**
- **Very Low Noise (30 pJ/cm^2 Noise Equivalent Illumination)**
- **Antiblooming**
- **Exposure Control**
- **20-lead 0.4" DIL Package**
- **Electrical, Mechanical and Optical Compatibility Between the Two Products**

2. Applications

The TH7813 and TH7814 linear arrays are based on e2v's know-how in terms of design and technology. Flexibility and performance of these devices give the opportunity to use them in most vision systems for industrial applications (web inspection, process control, sorting and inspection of various parts), document scanning up to 200 dpi, metrology, etc.

Figure 2-1. Block Diagram



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3. Pin Identification

All pins must be connected.

Figure 3-1. Package Top View

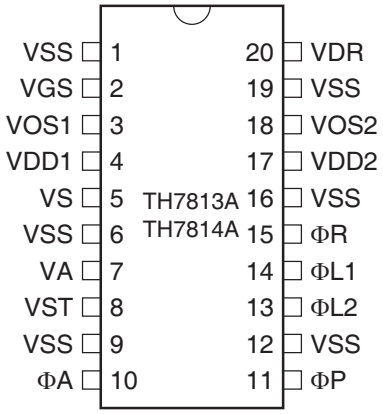

Table 3-1. Pin Description

Pin Number	Symbol	Function
4, 17	VDD1,2	Output amplifiers drain supply
3, 18	VOS1,2	Video outputs
5	VS	Output amplifiers substrate bias
20	VDR	Reset drain bias
2	VGS	Output gate bias
14	ΦL1	Readout register clocks
13	ΦL2	
15	ΦR	Reset clock
10	ΦA	Antiblooming gate bias/clock
7	VA	Antiblooming drain bias
8	VST	Storage gate bias
11	ΦP	Transfer gate clock
1, 6, 9, 12, 16, 19	VSS	Ground, optical shield grounding (internally connected)

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4. Absolute Maximum Ratings

Table 4-1. Absolute Maximum Ratings(*NOTICE:)

Storage Temperature Range ..... -55°C to +150°C
Operating Temperature Range ..... -40°C to +85°C
Thermal Cycling.....15°C/mn
Maximum Applied Voltages:
• Pin: 2, 8, 10, 11, 13, 14, 15 ..... -0.3 to 15V
• Pin: 4, 5, 7, 17, 20 ..... -0.3 to 16V
• Pin: 1, 6, 9, 12, 16, 19 .....0V (ground)

*NOTICE: Stresses above those listed under absolute maximum ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

5. Operating Range and Operating Precautions

Operating range defines the limits within which the functionality is guaranteed. Electrical limits of applied signals are given in Section 6.

Shorting the video outputs to any other pin, even temporarily, can permanently damage the on-chip output amplifier.

6. Operating Conditions

Table 6-1. DC Characteristics

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Output Amplifier Drain Supply	VDD1, VDD2	14.5	15	15.5	V
Storage Gate Bias	VST	2.2	2.4	2.6	V
Antiblooming Diode Bias	VA	14.5	15	15.5	V
Reset Bias	VDR	13.5	14	14.5	V
Antiblooming Diode Bias	VA	14.5	15	15.5	V
Register Output Gate Bias	VGS	2.2	2.4	2.6	V
Output Amplifier Source Supply	VS		0		V
Ground	VSS		0		

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Table 6-2. Drive Clocks Characteristics

Parameter	Symbol	Value			Unit	Comment
		Min	Typ	Max		
Reset gate	ΦR					
High level		8.5	9	9.5	V	Clock Capacitance < 25 pF
Low level		-0.1	0	0.4	V	
Transfer gate	ΦP					
High level		8.5	9	9.5	V	Clock Capacitance < 100 pF
Low level		-0.1	0	0.4	V	
Readout register clocks	ΦL1, 2					
High level		8.5	9	9.5	V	see Figure 7-1 and Figure 7-2
Low level		-0.1	0	0.4	V	
Readout register frequency	F_H	—	10	25	MHz	
Antiblooming gate	φA	0	0	0	V	If antiblooming operation inhibited
		See Table 9-1 on page 8				Exposure time reduction
		See Figure 10-1 on page 9				Pixel saturation adjustment

7. Clock Capacitances

Figure 7-1. Readout Register Clocks Capacitance TH7813

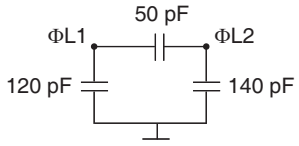
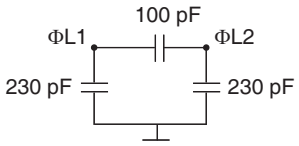


Figure 7-2. Readout Register Clocks Capacitance TH7814



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7.1 Timing Diagrams

The following diagram shows the general clocking scheme for the TH7813A and TH7814A.

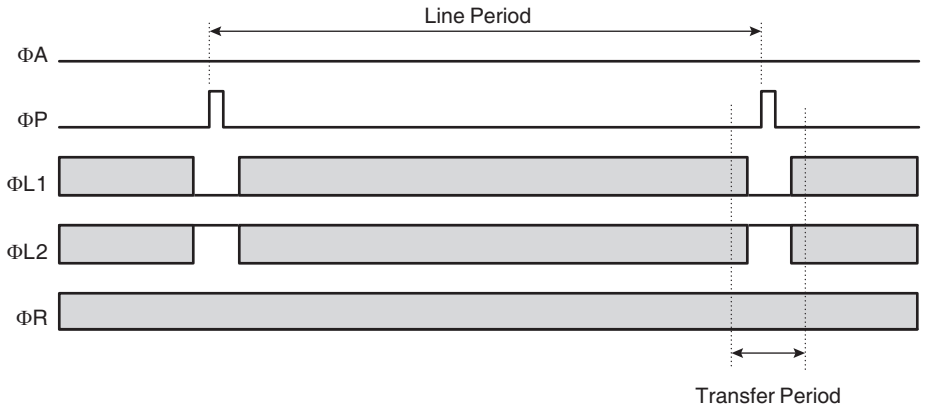
The line is composed as follows:

Synopsis	Number of Prescan Pixels per Output	Number of Useful Pixels per Output	Total Number of Pixels per Output
TH7813A	4	512	516
TH7814A	4	1024	1028

Postscan elements may be added in order to either increase the exposure time, or to provide a voltage reference level.

The following diagram shows the timing for the transfer period.

Figure 7-3. Line Timing Diagram



ΦR clock may also be held in high state during line transfer period.

Figure 7-4. Line Transfer Period

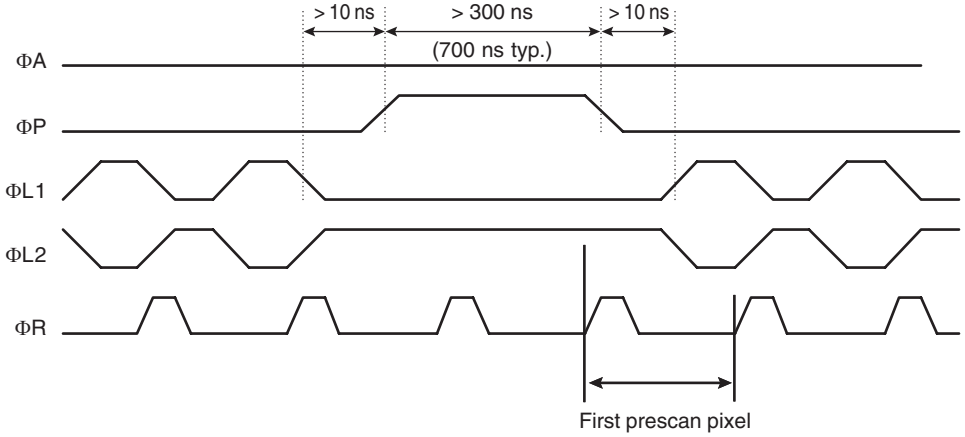


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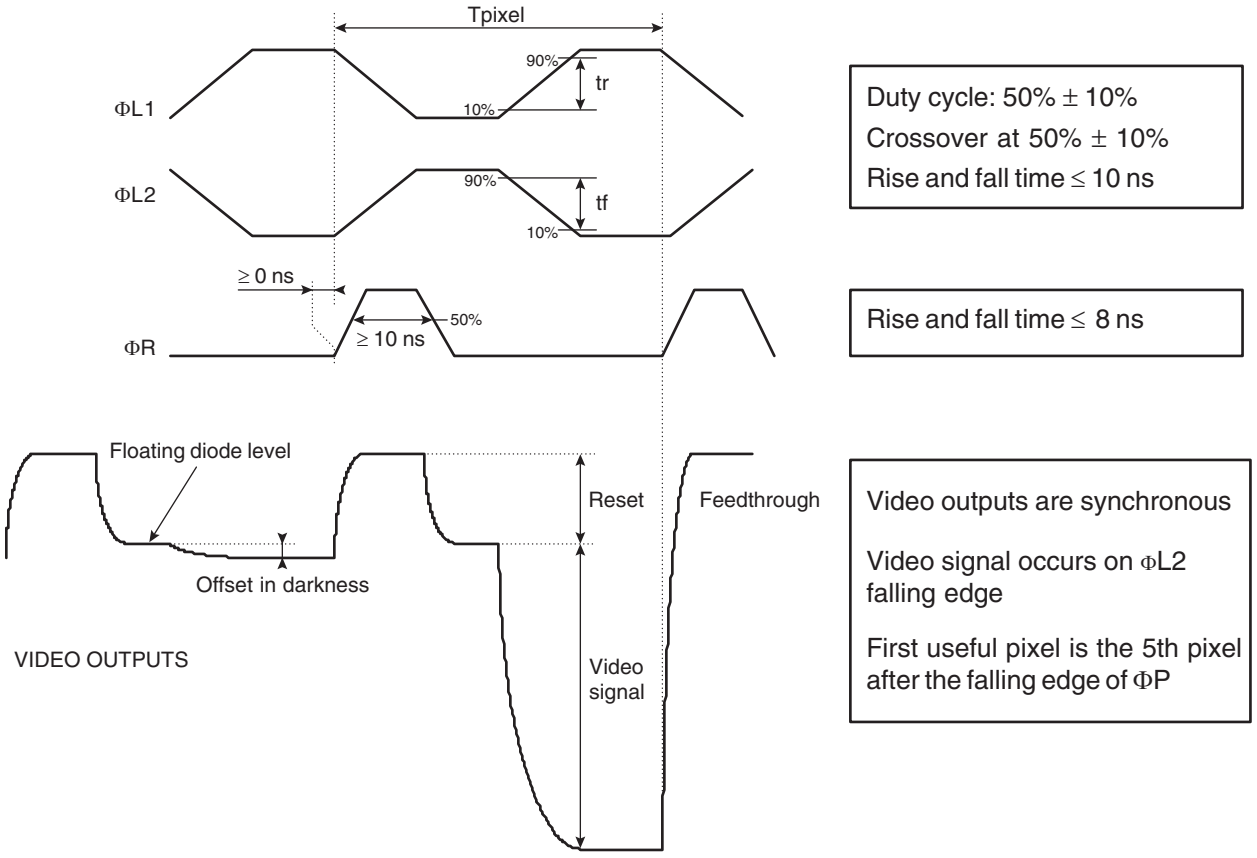
Diagram Figure 7-5 shows the detailed timing for the pixel readout:

Figure 7-5. Pixel Readout Timing Diagram



7.2 Exposure Time Reduction

The antiblooming structure of the TH7813A and TH7814A provides an electronic shutter capability by clocking phase ϕA during the line period. The timing diagram is described below:

Antiblooming Gate	ΦA	Min	Typ	Max	Unit	Clock Capacitance (1)
High Level		8.5	9	9.5	V	Low Level Sets Saturation Level
Low Level		2	4	7	V	See Pixel Saturation Adjustment

Note: 1. ΦA Clock capacitance: TH7813A = 50 pF, TH7814A = 100 pF

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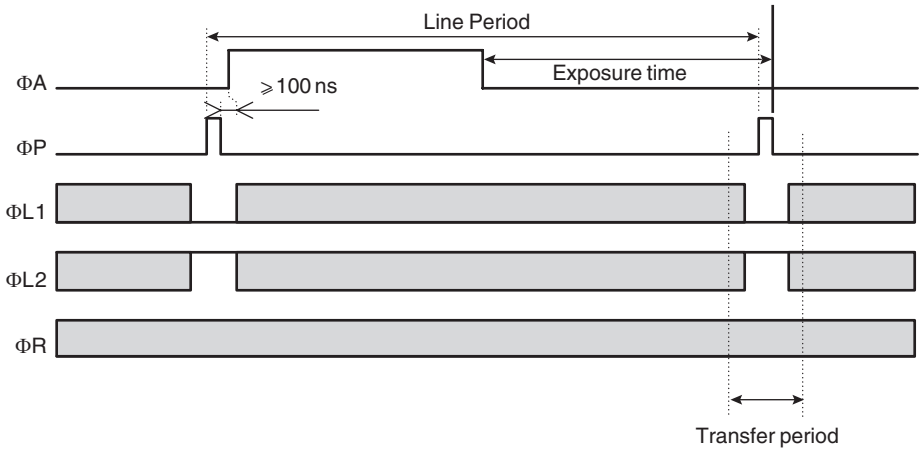
Figure 1. Exposure Time Reduction



8. Electrical Performance

Table 8-1. Static and Dynamic Electrical Characteristics

Parameter	Symbol	Value			Unit	Comments
		Min	Typ	Max		
Output Amplifier Supply Current	I_{DD}		10		mA	per amplifier
Output Impedance	Z_S	200	225	250	Ω	
DC Output Level	V_{REF}		10		V	
Output Conversion Factor	CVF		5		µV/e-	
Offset in Darkness	DC off		30		mV	
Reset Feedthrough	Vft		400		mV	
CTF	CTF		65		%	
LAG	LAG			1	%	$\overline{VOS}$ > 50 mV
Charge Transfer Inefficiency (per stage)	HCTI			8.10^{-5}		

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9. Electro-optical Performance

- General test conditions:
  - T_{CASE} = 25°C
  - Light source: 2854K with 2 mm BG38 filter (unless specified) + F/11 optical aperture
  - Typical operating conditions: 2 x 10 MHz
- All values are referred to prescan pixels level

Table 9-1. Electro-optical Performance Characteristics

Parameter	Symbol	Value			Unit	Comments
		Min	Typ	Max		
Saturation Output Voltage	V_{SAT}	1.65	2	3	V	VΦA = 0V
Responsivity	R	7.5	8.5		V/µJ/cm^2	
Responsivity Unbalance			0.5%	5	%	
Photo Response Non Uniformity Peak-to-peak	PRNU		±5	±10	%V_{OS}	$\overline{VOS}$ = 50 mV to 1.5V
Dark Signal	DS		0.1	0.4	mV/ms	Depends on integration time ms
Dark Signal Non Uniformity (1σ)	DSNU			0.1	mV/ms	Depends on integration time ms
Temporal RMS Noise in Darkness	V_N		300		µV	
Dynamic Range	DR	5,500	6,600			
CTF	CTF		65		%	
LAG	LAG			1	%	$\overline{VOS}$ > 50 mV
Charge Transfer Inefficiency (per stage)	HCTI			8.10^{-5}		

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10. Electro-optical Performances without Infrared Cut-off Filter

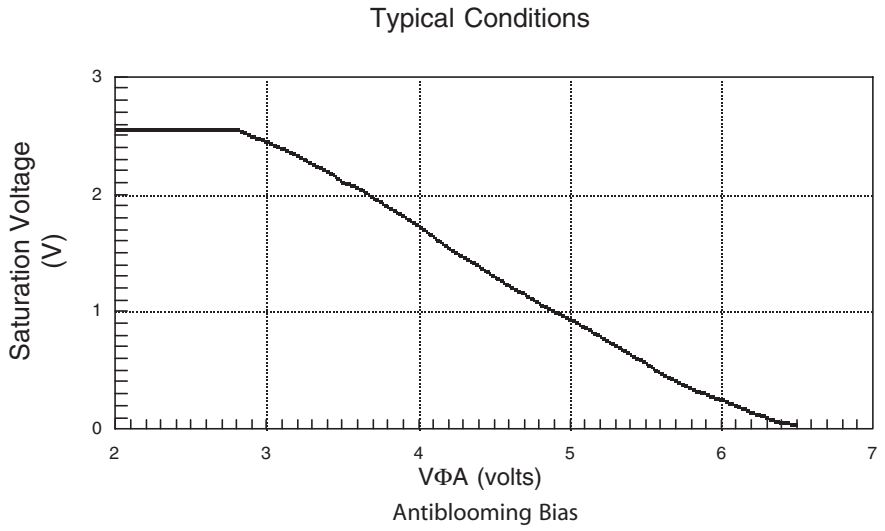
The TH7813A and TH7814A special semiconductor process enables to exploit the silicon's high near infrared sensitivity while maintaining good imaging performances in terms of response uniformity and resolution. Typical changes in performance with and without IR filtering are summarized below:

Parameter	With IR Cut-off Filter	Without IR Cut-off Filter
Average Video Signal Due to a Given Illumination	V_{OS}	6 x V_{OS}
PRNU (Single Defects Excluded)	±5%	5%
CTF at Nyquist Frequency	65%	40%

10.1 Pixel Saturation Adjustment

The TH7813A and TH7814A antiblooming structure can be used to adjust the maximum saturation voltage, by adjusting the ΦA bias voltage. The following curve shows the relation between V_{SAT} and VΦA.

Figure 10-1. Pixel Saturation versus Antiblooming ΦA Low Level (Typical Conditions)



11. Spectral Responsivity

The following curve shows the typical responsivity for TH7813A and TH7814A.

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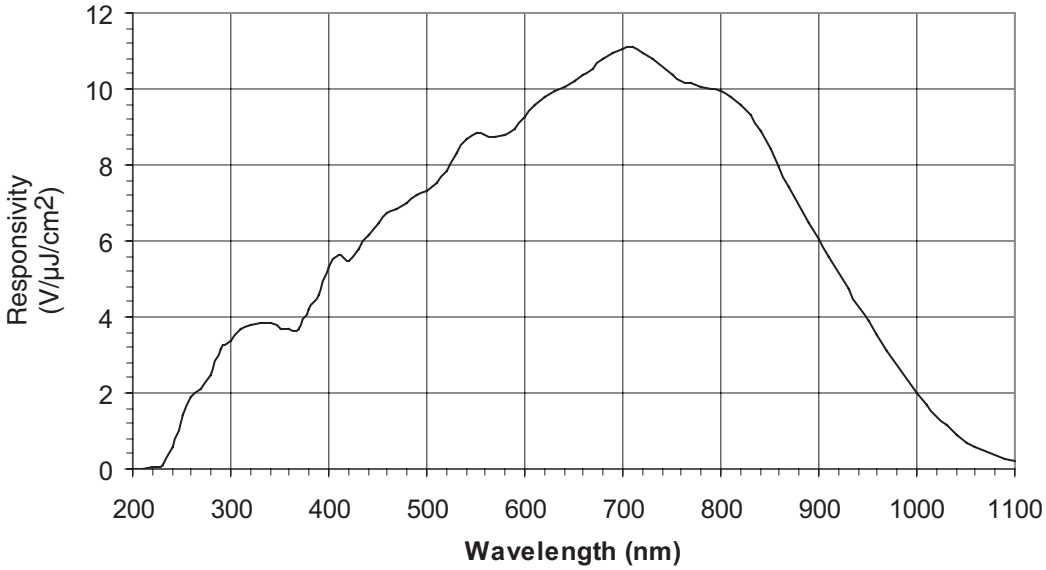
Figure 11-1. Spectral Responsivity



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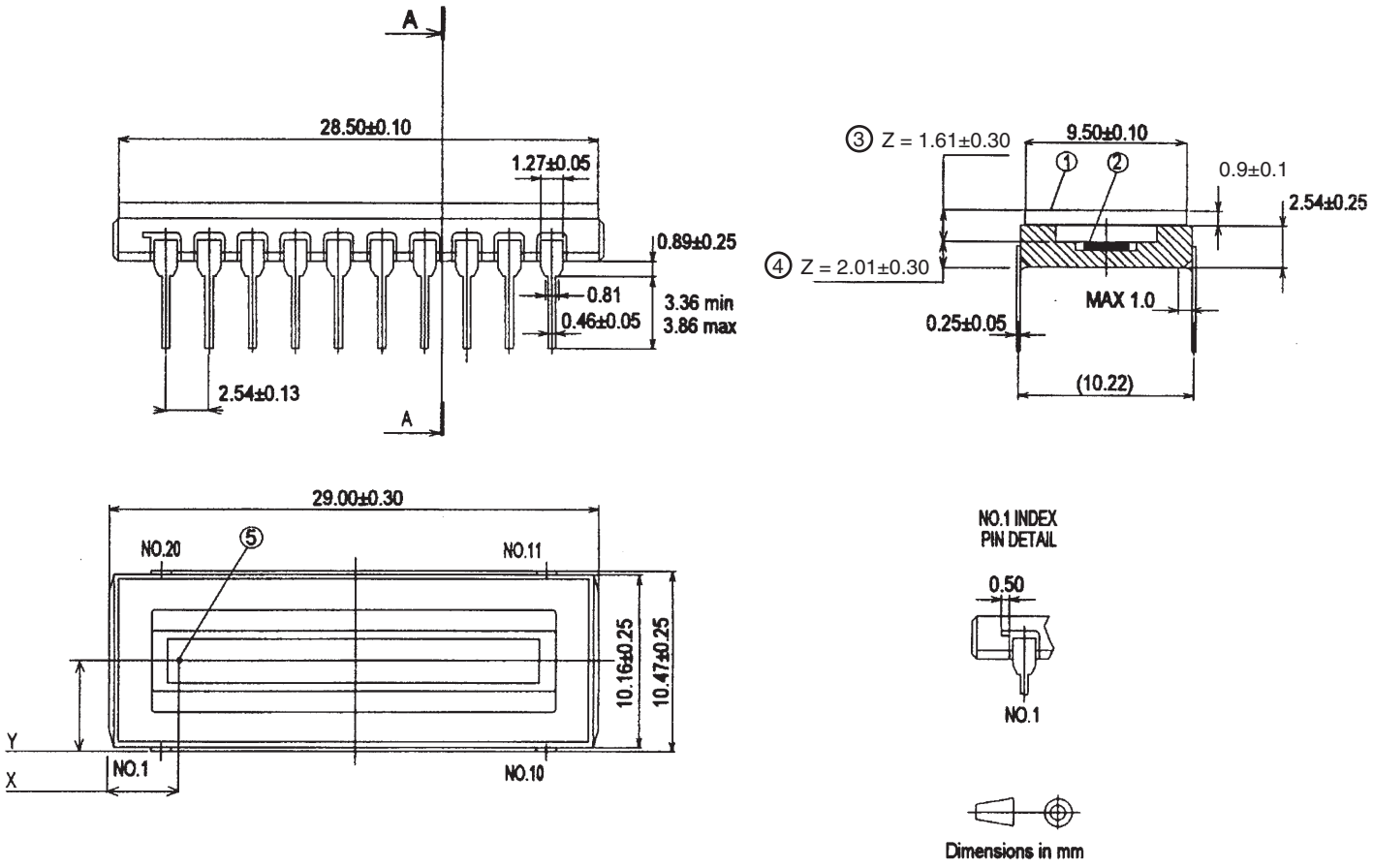
11.1 Package Information

Both devices have the same optical center.

Figure 11-2. Package Outline



Notes:
1. Window
2. Photosensitive area
3. Optical distance between external face of window and photosensitive area
4. Optical distance between backside of package and photosensitive area
5. First pixel position (mm):

TH7813A	TH7814A
X = 9.6 ± 0.4	X = 4.5 ± 0.4
Y = 5.2 ± 0.35	Y = 5.2 ± 0.35

11.2 Ordering Code

- TH7813ACC
- TH7814ACC

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