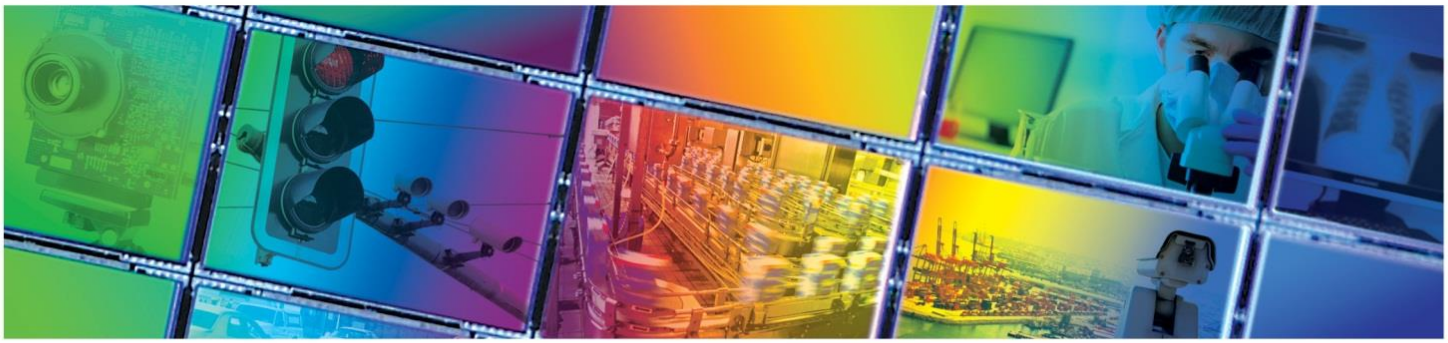
ON Semiconductor®

KAI-11002 IMAGE SENSOR

4008 (H) X 2672 (V) INTERLINE CCD IMAGE SENSOR



JUNE 4, 2014

DEVICE PERFORMANCE SPECIFICATION

REVISION 1.1 PS-0012

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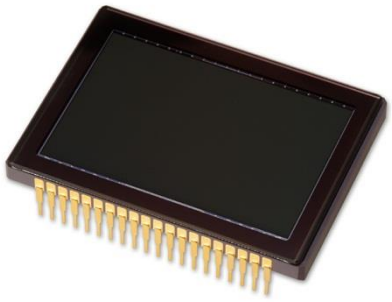
KAI-11002 Image Sensor

DESCRIPTION

The KAI-11002 Image Sensor is a high-performance 11-million pixel sensor designed for professional digital still camera applications. The 9.0 µm square pixels with microlenses provide high sensitivity and the large full well capacity results in high dynamic range. The two high-speed outputs and binning capabilities allow for 1-3 frames per second (fps) video rate for the progressively scanned images. The vertical overflow drain structure provides antiblooming protection and enables electronic shuttering for precise exposure control. Other features include low dark current, negligible lag and low smear.



FEATURES

- High resolution
- High sensitivity
- High dynamic range
- Low noise architecture
- High frame rate
- Binning capability for higher frame rate
- Electronic shutter

APPLICATIONS

- Industrial Inspection
- Aerial Photography

Parameter	Value
Architecture	Interline CCD; Progressive Scan
Total Number of Pixels	4072 (H) x 2720 (V) = 11.1M
Number of Effective Pixels	4033 (H) x 2688 (V) = 10.8M
Number of Active Pixels	4008 (H) x 2672 (V) = 10.7M
Number of Outputs	1 or 2
Pixel Size	9.0 µm (H) x 9.0 µm (V)
Imager Size	43.3mm (diagonal)
Chip Size	37.25mm (H) x 25.70mm (V)
Aspect Ratio	3:2
Saturation Signal	60,000 electrons
Quantum Efficiency KAI-11002-ABA KAI-11002-CBA (RGB)	 50% 34%, 37%, 42%
Output Sensitivity	13 µV/e
Total Noise	30 electrons
Dark Current	< 50 mV/s
Dark Current Doubling Temperature	7 °C
Dynamic Range	66 dB
Charge Transfer Efficiency	> 0.99999
Blooming Suppression	> 1000X
Smear	< -80 dB
Image Lag	< 10 electrons
Maximum Data Rate	28 MHz
Package	40-pin, CerDIP, 0.070" pin spacing
Cover Glass	AR Coated

All parameters above are specified at T = 40 °C

Ordering Information

Catalog Number	Product Name	Description	Marking Code
4H0745	KAI-11002-AAA-CR-B1	Monochrome, No Microlens, CERDIP Package (sidebrazed), Taped Clear Cover Glass with AR coating (2 sides), Grade 1	KAI-11002-AAA S/N
4H0746	KAI-11002-AAA-CR-B2	Monochrome, No Microlens, CERDIP Package (sidebrazed), Taped Clear Cover Glass with AR coating (2 sides), Grade 2	
4H0747	KAI-11002-AAA-CR-AE	Monochrome, No Microlens, CERDIP Package (sidebrazed), Taped Clear Cover Glass with AR coating (2 sides), Engineering Sample	
4H0805	KAI-11002-ABA-CD-BX	Monochrome, Telecentric Microlens, CERDIP Package (sidebrazed), Clear Cover Glass with AR coating (both sides), Special Grade	KAI-11002-ABA S/N
4H0735	KAI-11002-ABA-CD-B0	Monochrome, Telecentric Microlens, CERDIP Package (sidebrazed), Clear Cover Glass with AR coating (both sides), Grade 0	
4H0736	KAI-11002-ABA-CD-B1	Monochrome, Telecentric Microlens, CERDIP Package (sidebrazed), Clear Cover Glass with AR coating (both sides), Grade 1	
4H0737	KAI-11002-ABA-CD-B2	Monochrome, Telecentric Microlens, CERDIP Package (sidebrazed), Clear Cover Glass with AR coating (both sides), Grade 2	
4H0738	KAI-11002-ABA-CD-AE	Monochrome, Telecentric Microlens, CERDIP Package (sidebrazed), Clear Cover Glass with AR coating (both sides), Engineering Sample	
4H0742	KAI-11002-ABA-CR-B1	Monochrome, Telecentric Microlens, CERDIP Package (sidebrazed), Taped Clear Cover Glass with AR coating (2 sides), Grade 1	
4H0743	KAI-11002-ABA-CR-B2	Monochrome, Telecentric Microlens, CERDIP Package (sidebrazed), Taped Clear Cover Glass with AR coating (2 sides), Grade 2	
4H0744	KAI-11002-ABA-CR-AE	Monochrome, Telecentric Microlens, CERDIP Package (sidebrazed), Taped Clear Cover Glass with AR coating (2 sides), Engineering Sample	
4H0732	KAI-11002-CAA-CD-B1	Color (Bayer RGB), No Microlens, CERDIP Package (sidebrazed), Clear Cover Glass with AR coating (both sides), Grade 1	KAI-11002-CAA S/N
4H0733	KAI-11002-CAA-CD-B2	Color (Bayer RGB), No Microlens, CERDIP Package (sidebrazed), Clear Cover Glass with AR coating (both sides), Grade 2	
4H0734	KAI-11002-CAA-CD-AE	Color (Bayer RGB), No Microlens, CERDIP Package (sidebrazed), Clear Cover Glass with AR coating (both sides), Engineering Sample	
4H0739	KAI-11002-CBA-CD-B1	Color (Bayer RGB), Telecentric Microlens, CERDIP Package (sidebrazed), Clear Cover Glass with AR coating (both sides), Grade 1	KAI-11002-CBA S/N
4H0740	KAI-11002-CBA-CD-B2	Color (Bayer RGB), Telecentric Microlens, CERDIP Package (sidebrazed), Clear Cover Glass with AR coating (both sides), Grade 2	
4H0741	KAI-11002-CBA-CD-AE	Color (Bayer RGB), Telecentric Microlens, CERDIP Package (sidebrazed), Clear Cover Glass with AR coating (both sides), Engineering Sample	
4H0178	KEK-4H0178-KAI-11000/11002-12-30	Evaluation Board (Complete Kit)	n/a

See Application Note *Product Naming Convention* for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.truesenseimaging.com.

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Device Description

ARCHITECTURE

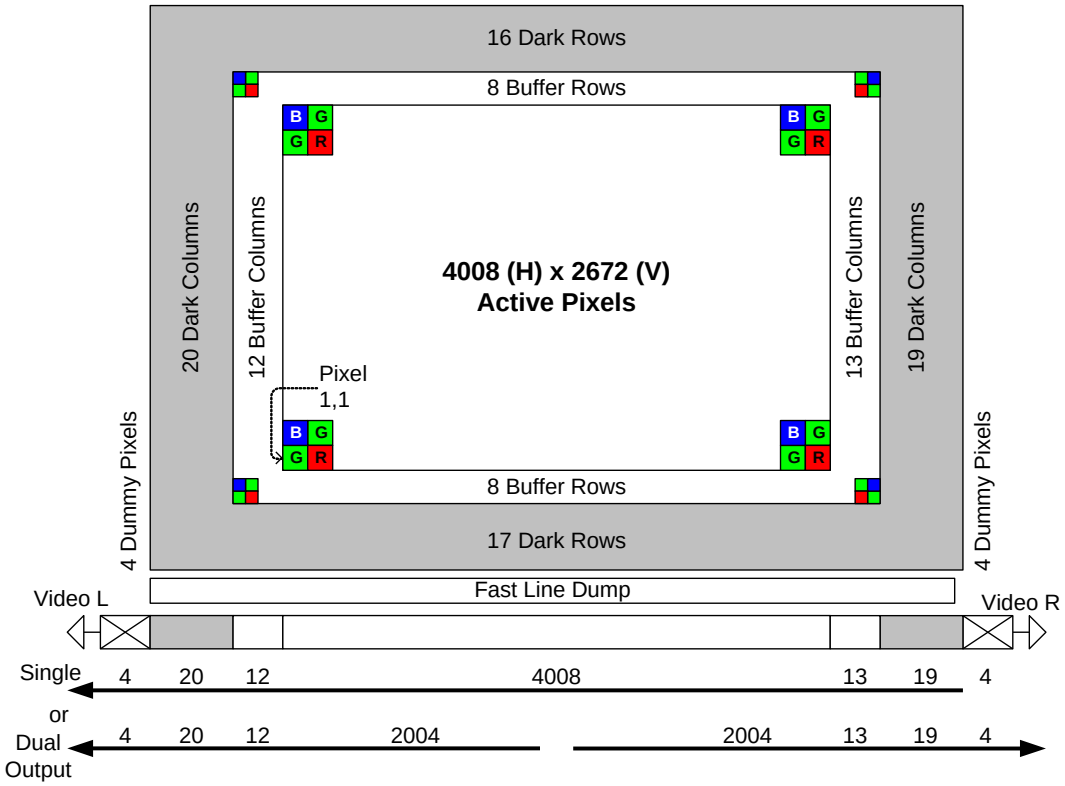


Figure 1: Block Diagram

There are 17 light shielded rows followed 2688 photoactive rows and finally 16 more light shielded rows. The first 8 and the last 8 photoactive rows are buffer rows giving a total of 2672 lines of image data.

In the single output mode all pixels are clocked out of the Video L output in the lower left corner of the sensor. The first 4 empty pixels of each line do not receive charge from the vertical shift register. The next 20 pixels receive charge from the left light shielded edge followed by 4033 photosensitive pixels and finally 19 more light shielded pixels from the right edge of the sensor. The first 12 and last 13 photosensitive pixels are buffer pixels giving a total of 4008 pixels of image data.

In the dual output mode the clocking of the right half of the horizontal CCD is reversed. The left half of the image is clocked out Video L and the right half of the image is clocked out Video R. For the Video L each row consists of 4 empty pixels followed by 20 light shielded pixels followed by 2016 photosensitive pixels. For the Video R each row consists of 4 empty pixels followed by 19 light shielded pixels followed by 2017 photosensitive pixels. When reconstructing the image, data from Video R will have to be reversed in a line buffer and appended to the Video L data.

The dark rows are not entirely dark and so should not be used for a dark reference level. Use the dark columns on the left or right side of the image sensor as a dark reference.

Of the dark columns, the first and last dark columns should not be used for determining the zero signal level. Some light does leak into the first and last dark columns.

PIXEL

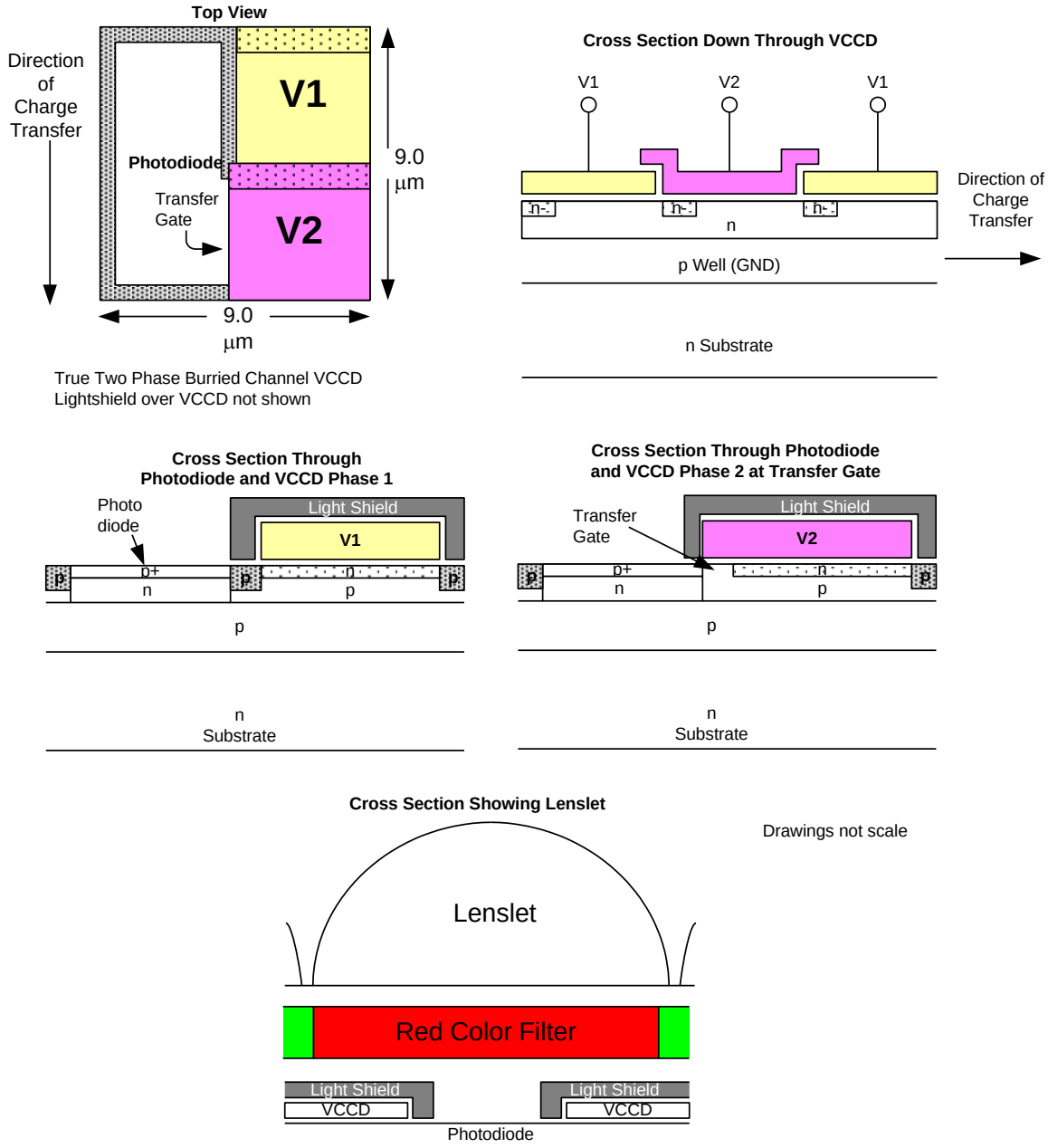


Figure 2: Pixel Architecture

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron-hole pairs within the individual silicon photodiodes. These photoelectrons are collected locally by the formation of potential wells at each photosite. Below photodiode saturation, the number of photoelectrons collected at each pixel is linearly dependent upon light level and exposure time and non-linearly dependent on wavelength. When the photodiodes charge capacity is reached, excess electrons are discharged into the substrate to prevent blooming.

VERTICAL TO HORIZONTAL TRANSFER

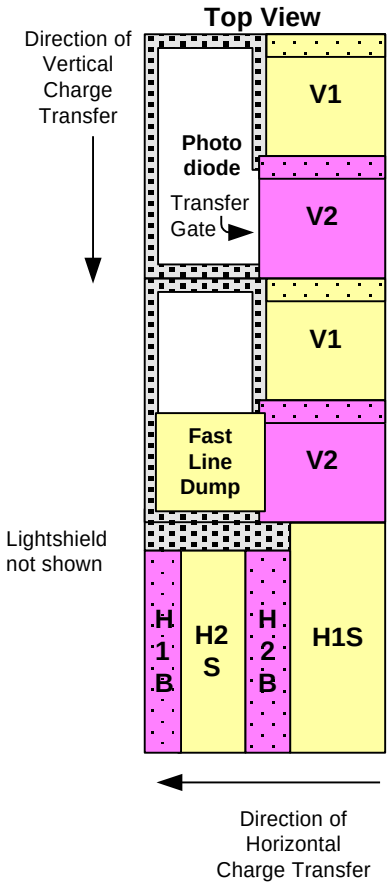


Figure 3: Vertical to Horizontal Transfer Architecture

When the V1 and V2 timing inputs are pulsed, charge in every pixel of the VCCD is shifted one row towards the HCCD. The last row next to the HCCD is shifted into the HCCD. When the VCCD is shifted, the timing signals to the HCCD must be stopped. H1 must be stopped in the high state and H2 must be stopped in the low state. The HCCD clocking may begin T_{HD} µs after the falling edge of the V1 and V2 pulse.

Charge is transferred from the last vertical CCD phase into the H1S horizontal CCD phase. Refer to Figure 25 for an example of timing that accomplishes the vertical to horizontal transfer of charge.

If the fast line dump is held at the high level (FDH) during a vertical to horizontal transfer, then the entire line is removed and not transferred into the horizontal register.

HORIZONTAL REGISTER TO FLOATING DIFFUSION

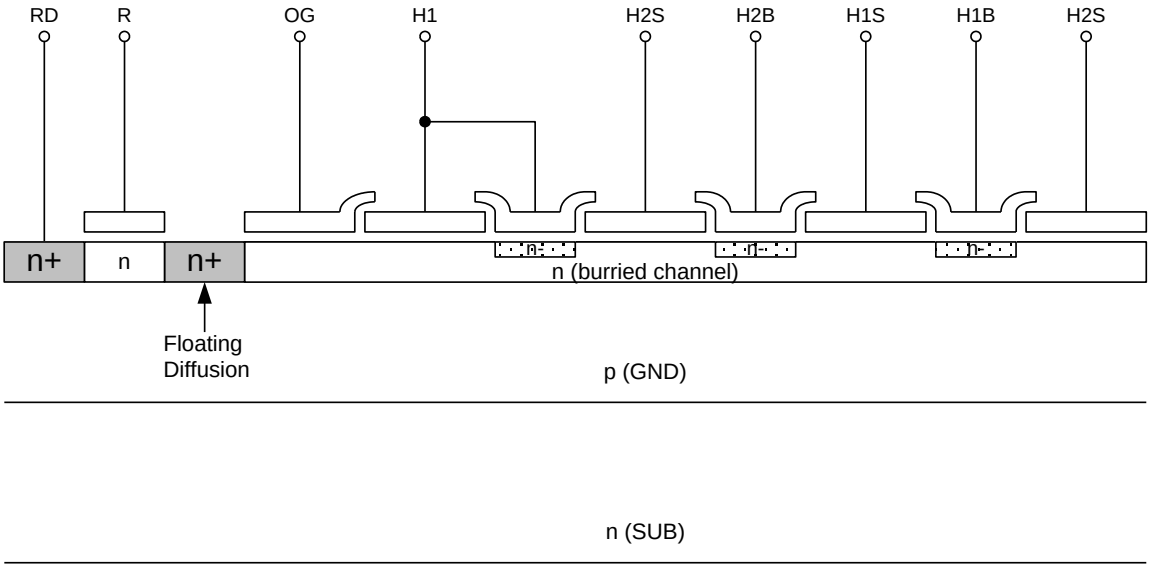


Figure 4: Horizontal Register to Floating Diffusion Architecture

The HCCD has a total of 4080 pixels. The 4072 vertical shift registers (columns) are shifted into the center 4072 pixels of the HCCD. There are 4 pixels at both ends of the HCCD, which receive no charge from a vertical shift register. The first 4 clock cycles of the HCCD will be empty pixels (containing no electrons). The next 20 clock cycles will contain only electrons generated by dark current in the VCCD and photodiodes. The next 4033 clock cycles will contain photo-electrons (image data). Finally, the last 19 clock cycles will contain only electrons generated by dark current in the VCCD and photodiodes. Of the 20 dark columns at the start of the line and the 19 dark columns at the end of the line, the first and last dark columns should not be used for determining the zero signal level. Some light does leak into the first and last dark columns. Only use the center 18 columns of the 20 column dark reference at the start of the line. Only use the center 17 columns of the 19 column dark reference at the end of the line.

When the HCCD is shifting valid image data, the timing inputs to the electronic shutter (SUB), VCCD (V1, V2), and fast line dump (FD) should be not be pulsed. This prevents unwanted noise from being introduced. The HCCD is a type of charge coupled device known as a pseudo-two phase CCD. This type of CCD has the ability to shift charge in two directions. This allows the entire image to be shifted out to the video L output, or to the video R output (left/right image reversal). The HCCD is split into two equal halves of 2040 pixels each. When operating the sensor in single output mode the two halves of the HCCD are shifted in the same direction. When operating the sensor in dual output mode the two halves of the HCCD are shifted in opposite directions. The direction of charge transfer in each half is controlled by the H1BL, H2BL, H1BR, and H2BR timing inputs.

HORIZONTAL REGISTER SPLIT

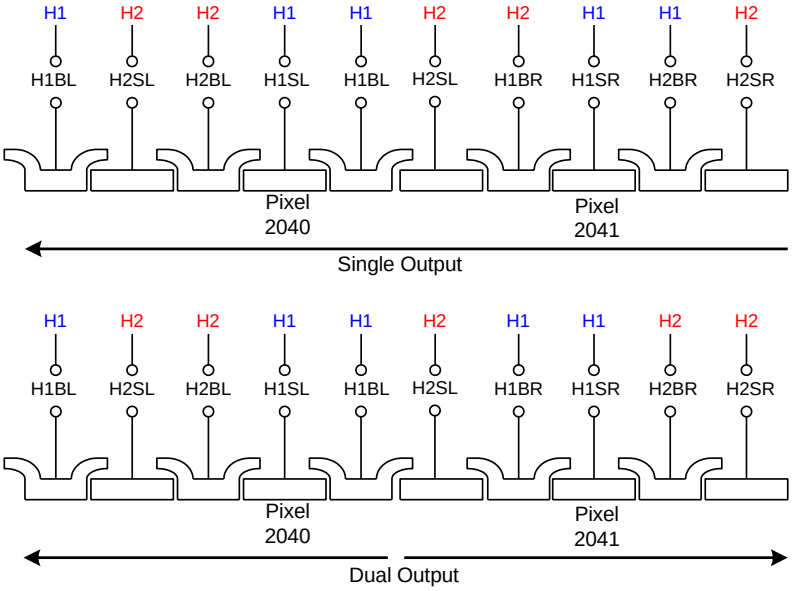


Figure 5: Horizontal Register

Single Output Operation

When operating the sensor in single output mode all pixels of the image sensor will be shifted out the Video L output (pin 2). To conserve power and lower heat generation the output amplifier for Video R may be turned off by connecting VDDR (pin 18) and VOUTR (pin 19) to GND (zero volts).

The H1 timing from the timing diagrams should be applied to H1SL, H1BL, H1SR, H2BR, and the H2 timing should be applied to H2SL, H2BL, H2SR, and H1BR. In other words, the clock driver generating the H1 timing should be connected to pins 8, 9, 13, and 11. The clock driver generating the H2 timing should be connected to pins 7, 10, 14, and 12. The horizontal CCD should be clocked for 4 empty pixels plus 20 light shielded pixels plus 4032 photoactive pixels plus 20 light shielded pixels for a total of 4076 pixels. H1BINL and H1BINR use the H1 timing, but should be generated from a separate clock driver for optimal performance.

Dual Output Operation

In dual output mode the connections to the H1BR and H2BR pins are swapped from the single output mode to change the direction of charge transfer of the right side horizontal shift register. In dual output mode both VDDL and VDDR (pins 3, 18) should be connected to 15 V. The H1 timing from the timing diagrams should be applied to H1SL, H1BL, H1SR, H1BR, and the H2 timing should be applied to H2SL, H2BL, H2SR, and H2BR. The clock driver generating the H1 timing should be connected to pins 8, 9, 13, and 12. The clock driver generating the H2 timing should be connected to pins 7, 10, 14, and 11. The horizontal CCD should be clocked for 4 empty pixels plus 20 light shielded pixels plus 2016 photoactive pixels for a total of 2040 pixels. If the camera is to have the option of dual or single output mode, the clock driver signals sent to H1BR and H2BR may be swapped by using a relay. Another alternative is to have two extra clock drivers for H1BR and H2BR and invert the signals in the timing logic generator. If two extra clock drivers are used, care must be taken to ensure the rising and falling edges of the H1BR and H2BR clocks occur at the same time (within 3ns) as the other HCCD clocks.

OUTPUT

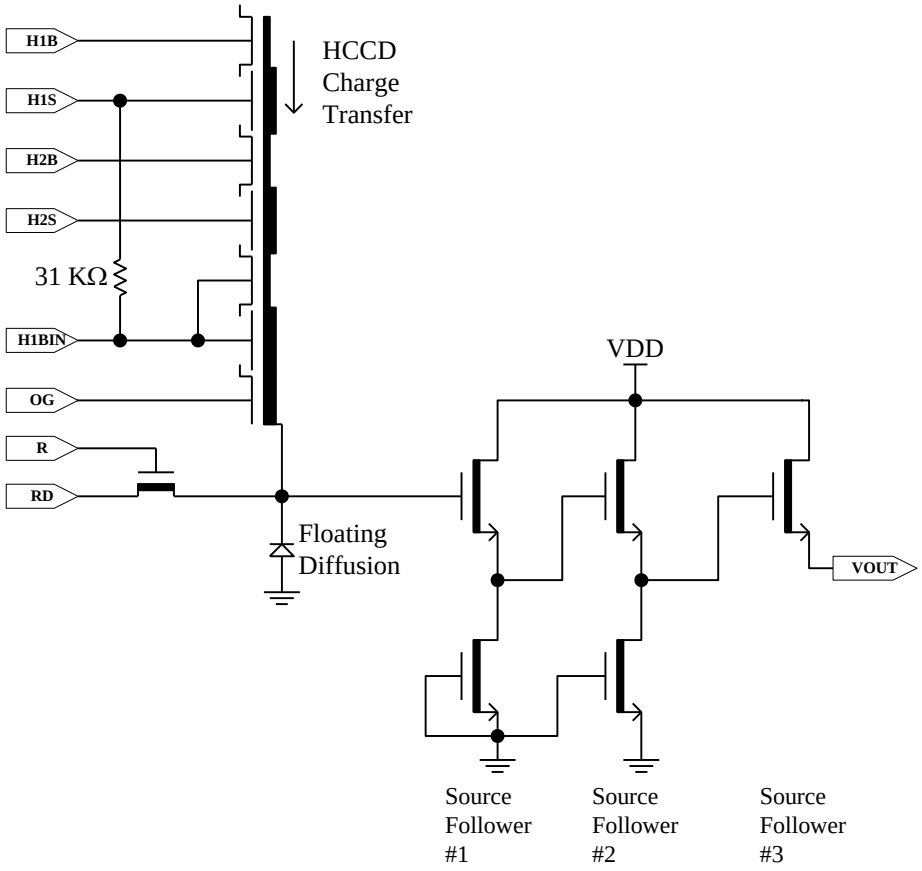


Figure 6: Output Architecture

Charge packets contained in the horizontal register are dumped pixel by pixel onto the floating diffusion (fd) output node whose potential varies linearly with the quantity of charge in each packet. The amount of potential charge is determined by the expression ΔVfd=ΔQ/Cfd. A three-stage source-follower amplifier is used to buffer this signal voltage off chip with slightly less than unity gain. The translation from the charge domain to the voltage domain is quantified by the output sensitivity or charge to voltage conversion in terms of microvolts per electron (μV/e^-). After the signal has been sampled off chip, the reset clock (R) removes the charge from the floating diffusion and resets its potential to the reset drain voltage (RD).

PIN DESCRIPTION AND PHYSICAL ORIENTATION

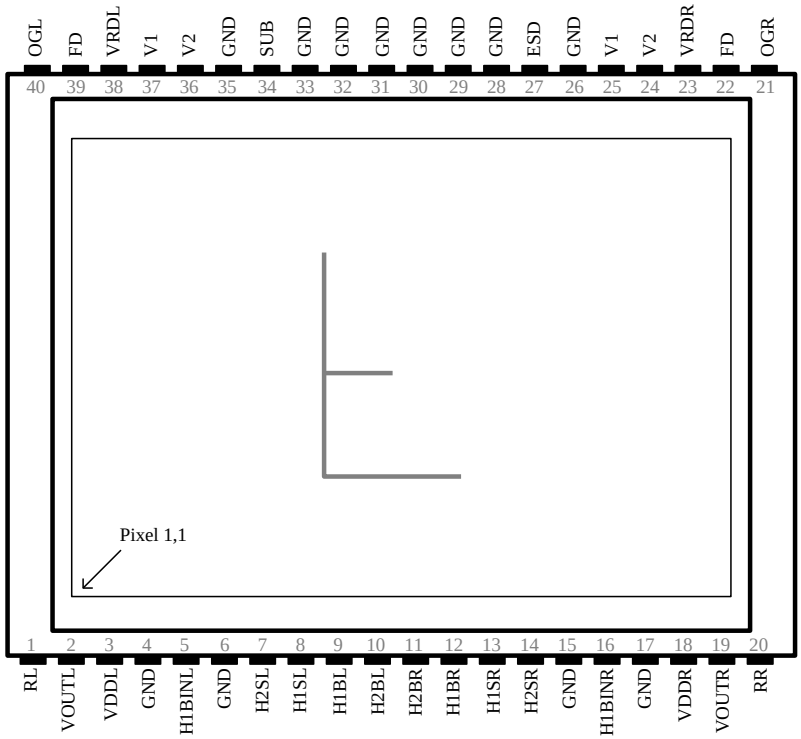


Figure 7: Pin Description

Pin	Name	Description
1	RL	Reset Gate, Left
2	VOUTL	Video Output, Left
3	VDDL	Vdd, Left
4	GND	Ground
5	H1BINL	H1 Last Phase, Left
6	GND	Ground
7	H2SL	H2 Storage, Left
8	H1SL	H1 Storage, Left
9	H1BL	H1 Barrier, Left
10	H2BL	H2 Barrier, Left
11	H2BR	H2 Barrier, Right
12	H1BR	H1 Barrier, Right
13	H1SR	H1 Storage, Right
14	H2SR	H2 Storage, Right
15	GND	Ground
16	H1BINR	H1 Last Phase, Right
17	GND	Ground
18	VDDR	Vdd, Right
19	VOUTR	Video Output, Right
20	RR	Reset Gate, Right

Pin	Name	Description
40	OGL	Output Gate, Left
39	FD	Fast Line Dump Gate
38	RDL	Reset Drain, Left
37	V1	Vertical Clock, Phase 1
36	V2	Vertical Clock, Phase 2
35	GND	Ground
34	SUB	Substrate
33	GND	Ground
32	GND	Ground
31	GND	Ground
30	GND	Ground
29	GND	Ground
28	GND	Ground
27	ESD	ESD Protection
26	GND	Ground
25	V1	Vertical Clock, Phase 1
24	V2	Vertical Clock, Phase 2
23	RDR	Reset Drain, Right
22	FD	Fast Line Dump Gate
21	OGR	Output Gate, Right

The pins are on a 0.070” spacing

Imaging Performance

IMAGING PERFORMANCE OPERATIONAL CONDITIONS

Unless otherwise noted, the Imaging Performance Specifications are measured using the following conditions.

Description	Condition	Notes
Frame Time	1732 msec	1
Horizontal Clock Frequency	10 MHz	
Light Source	Continuous red, green and blue illumination centered at 450, 530 and 650 nm	2,3
Operation	Nominal operating voltages and timing	

Notes:
1. Electronic shutter is not used. Integration time equals frame time.
2. LEDs used: Blue: Nichia NLPB500, Green: Nichia NSPG500S and Red: HP HLMP-8115.
3. For monochrome sensor, only green LED used.

SPECIFICATIONS

All Configurations

Description	Symbol	Min.	Nom.	Max.	Units	Sample Plan	Temperature Tested At (°C)	Notes
Maximum Photoresponse Nonlinearity	NL	n/a	2		%	Design		2, 3
Maximum Gain Difference Between Outputs	ΔG	n/a	10		%	Design		2, 3
Max. Signal Error due to Nonlinearity Dif.	ΔNL	n/a	1		%	Design		2, 3
Horizontal CCD Charge Capacity	HNe		139		ke^-	Design		
Vertical CCD Charge Capacity	VNe	90	91		ke^-	Die		
Photodiode Charge Capacity	PNe	58	60		ke^-	Die		
Horizontal CCD Charge Transfer Efficiency	HCTE	0.99999		n/a		Design		
Vertical CCD Charge Transfer Efficiency	VCTE	0.99999		n/a		Design		
Photodiode Dark Current	Ipd	n/a		800	e/p/s	Die	27, 40	
Photodiode Dark Current	Ipd	n/a		0.15	nA/cm^2	Die	27, 40	
Vertical CCD Dark Current	Ivd	n/a		3800	e/p/s	Die	27, 40	
Vertical CCD Dark Current	Ivd	n/a		0.5	nA/cm^2	Die	27, 40	
Image Lag	Lag	n/a	<10	50	e^-	Design		
Antiblooming Factor	Xab	100	300	n/a		Design		
Vertical Smear	Smr	n/a	-85	-75	dB	Design		
Total Noise	n_{e-T}		30		e^-rms	Design		4
Dynamic Range	DR		66		dB	Design		5
Output Amplifier DC Offset	V_{odc}	4	9	14	V	Die		
Output Amplifier Bandwidth	F_{-3db}		106		MHz	Die		6
Output Amplifier Impedance	R_{OUT}	100	150	200	Ohms	Die		
Output Amplifier Sensitivity	ΔV/ΔN		13		$\mu V/e^-$	Design		

KAI-11002-ABA Configuration

Description	Symbol	Min.	Nom.	Max.	Units	Sample Plan	Temperature Tested At (°C)	Notes
Peak Quantum Efficiency	QE_{max}	45	50	n/a	%	Design		
Peak Quantum Efficiency Wavelength	λQE	n/a	500	n/a	nm			

KAI-11002-CBA Configuration

Description		Symbol	Min.	Nom.	Max.	Units	Sample Plan	Temperature Tested At (°C)	Notes
Peak Quantum Efficiency	Red Green Blue	QE_{max}		34 37 42	n/a n/a n/a	%	Design		
Peak Quantum Efficiency Wavelength	Red Green Blue	λQE		630 550 470	n/a n/a n/a	nm	Design		

n/a: not applicable

Notes:
1. Per color.
2. Value is over the range of 10% to 90% of photodiode saturation.
3. Value is for the sensor operated without binning
4. Includes system electronics noise, dark pattern noise and dark current shot noise at 30 MHz.
5. Uses 20LOG(PNe/ n_{e-T})
6. Last stage only, Cload=10pF. Then $f_{-3db} = (1 / (2\pi * R_{out} * C_{load}))$

Typical Performance Curves

QUANTUM EFFICIENCY

Monochrome with Microlens

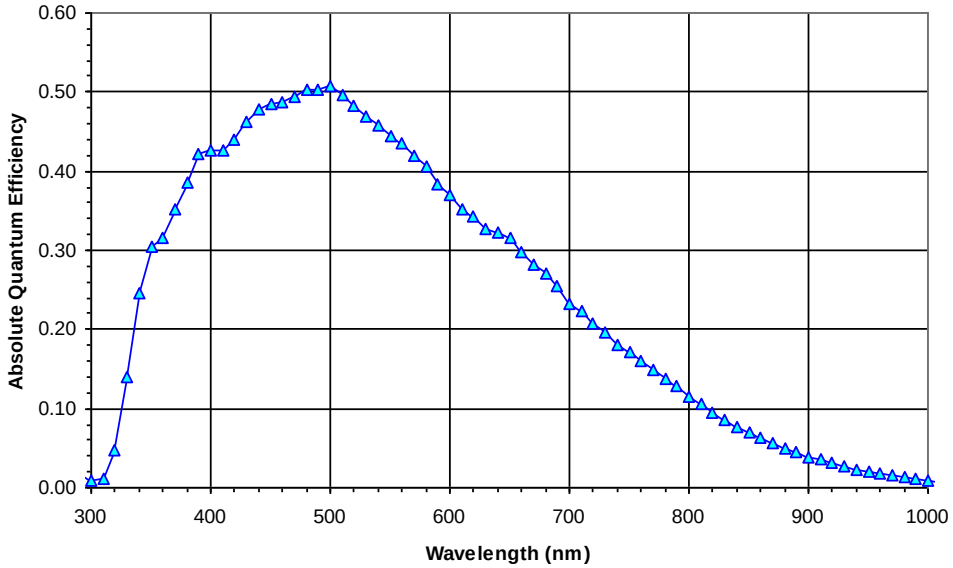


Figure 8: Monochrome with Microlens Quantum Efficiency

Monochrome without Microlens

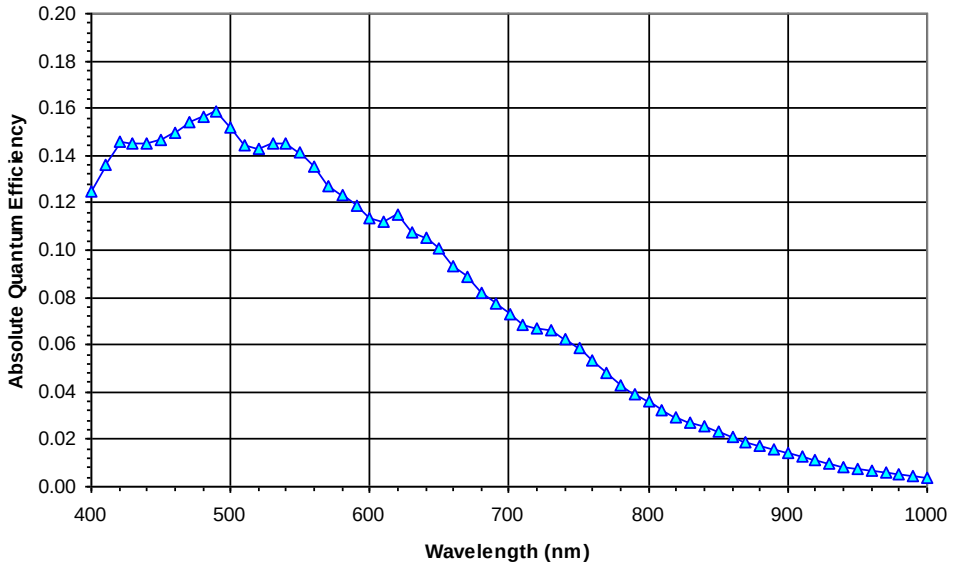


Figure 9: Monochrome without Microlens Quantum Efficiency

Color with Microlens

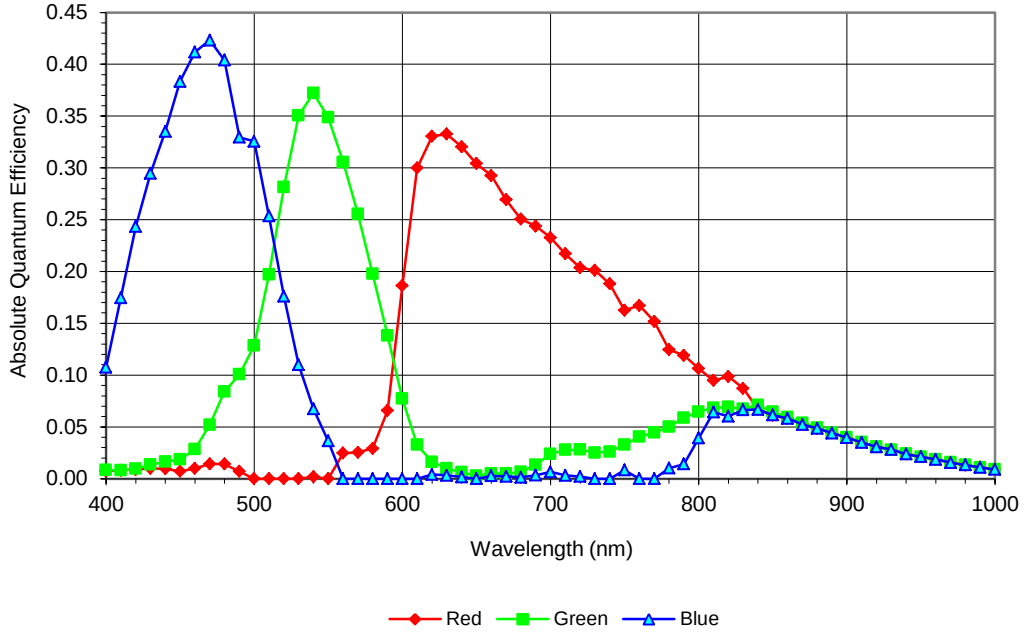


Figure 10: Color with Microlens Quantum Efficiency Using AR Glass

Color without Microlens

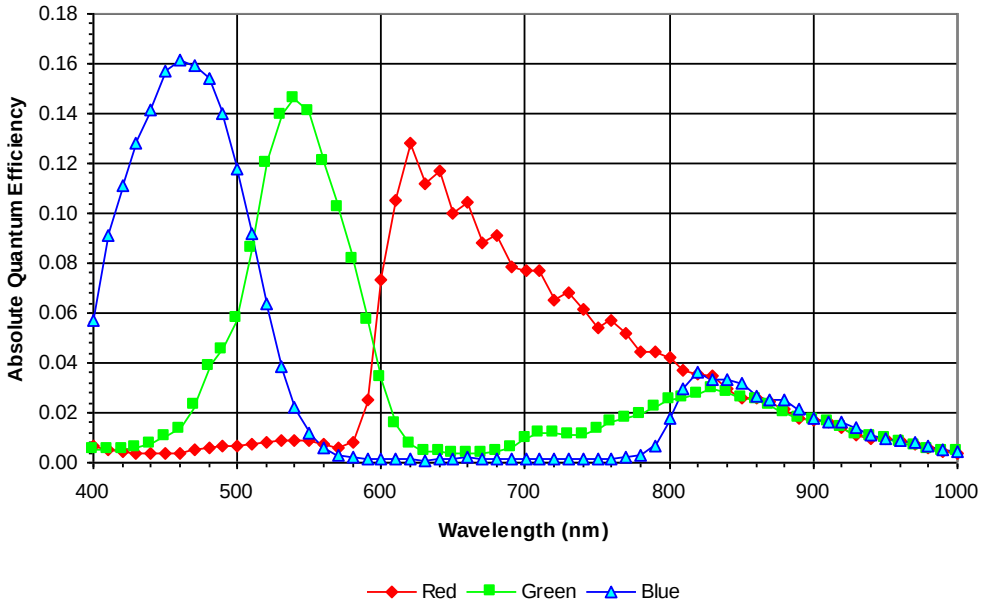


Figure 11: Color without Microlens Quantum Efficiency Using AR Glass

ANGULAR QUANTUM EFFICIENCY

For the curves marked “Horizontal”, the incident light angle is varied in a plane parallel to the HCCD.

For the curves marked “Vertical”, the incident light angle is varied in a plane parallel to the VCCD.

Monochrome with Microlens

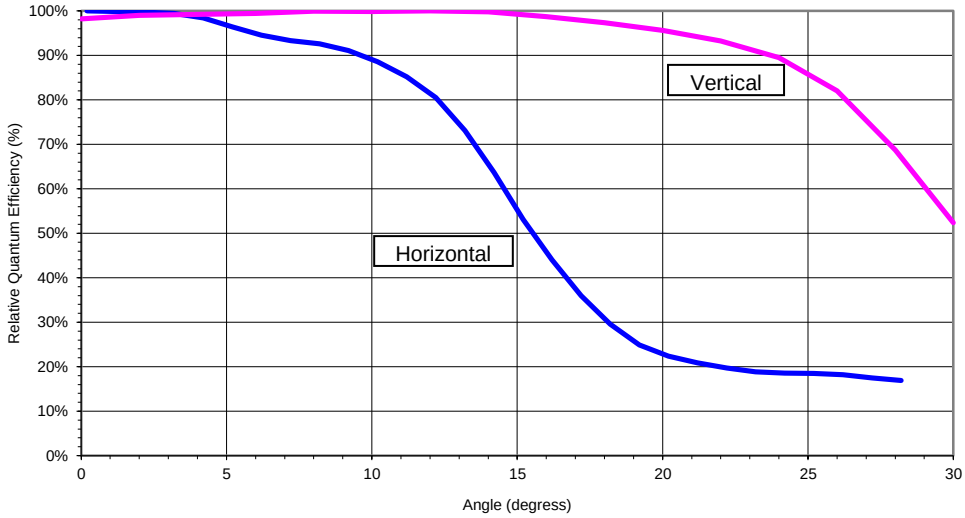


Figure 12: Monochrome with Microlens Angular Quantum Efficiency

Color with Microlens

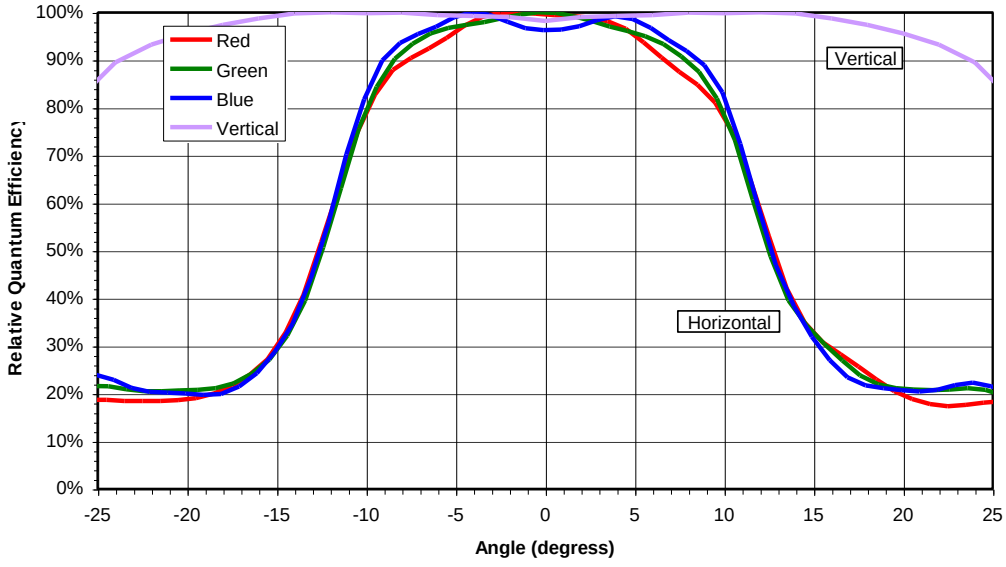


Figure 13: Color with Microlens Angular Quantum Efficiency

POWER - ESTIMATED

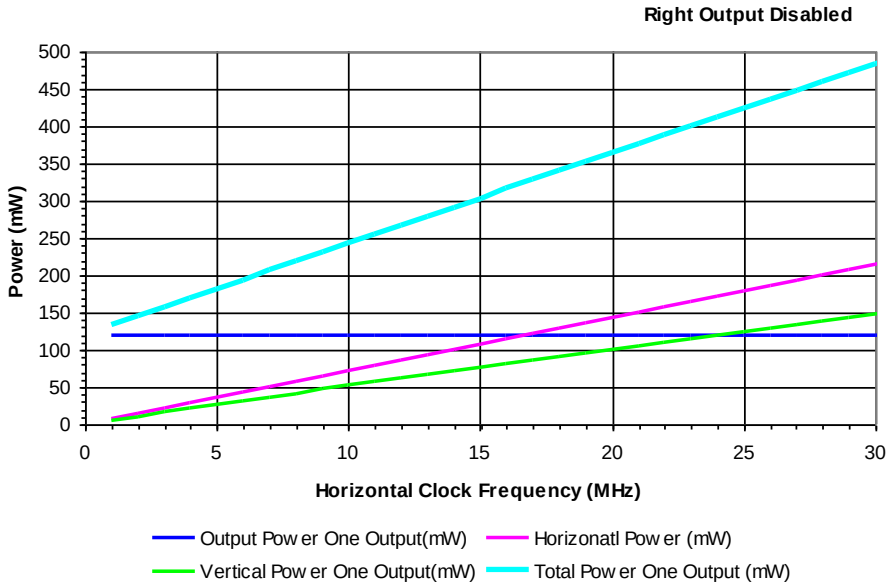


Figure 14: Power

FRAME RATES – CONTINUOUS MODE

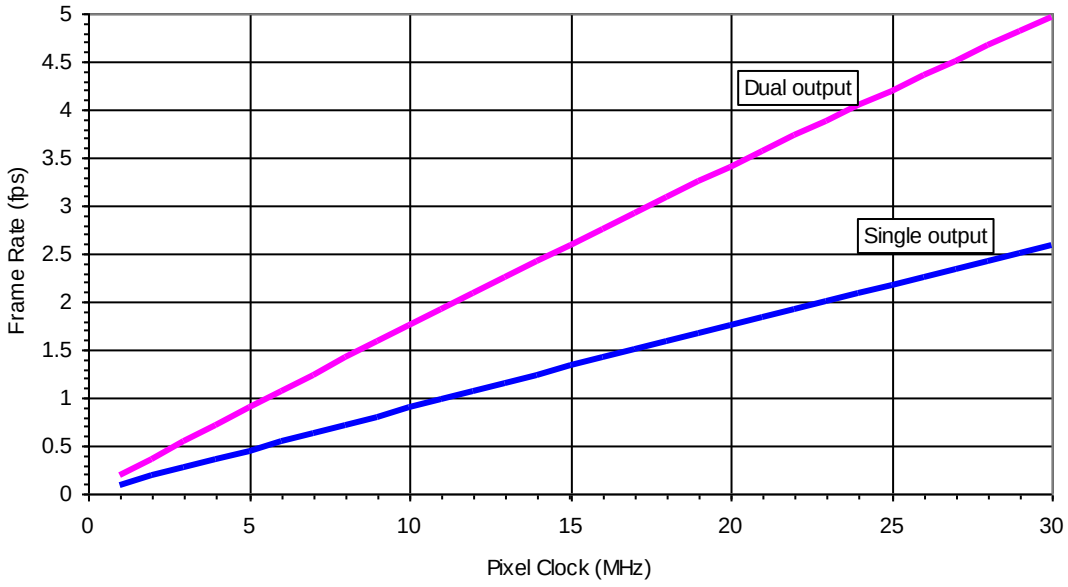


Figure 15: Frame Rates

Defect Definitions

Description	Definition	Class X Monochrome with microlens only	Class 0 Monochrome with microlens only	Class 1	Class 2 Color Only	Class 2 Monochrome Only	Notes
Major dark field defective pixel	Defect ≥ 239 mV	100	100	100	200	200	1,2
Major bright field defective pixel	Defect ≥ 15%						1,2
Minor dark field defective pixel	Defect ≥ 123 mV	1000	1000	1000	2000	2000	1,2
Cluster defect	A group of 2 to "N" contiguous major defective pixels, but no more than "W" adjacent defects horizontally	0	1 N=10 W=3	20 N=10 W=3	20 N=10 W=3	20 N=12 W=5	1,2
Column defect	A group of more than 10 contiguous major defective pixels along a single column	0	0	0	10	2	1,2

Notes:
1. There will be at least two non-defective pixels separating any two major defective pixels.
2. Tested at 27 °C and 40 °C.

Class X sensors are offered strictly "as available". Truesense Imaging cannot guarantee delivery dates. Please call for availability.

Defect Map

The defect map supplied with each sensor is based upon testing at an ambient (27 °C) temperature. Minor point defects are not included in the defect map. All defective pixels are reference to pixel 1,1 in the defect maps.

Test Definitions

Test Regions of Interest

Active Area ROI: Pixel (1, 1) to Pixel (4008, 2672)

Center 100 by 100 ROI: Pixel (1954, 1336) to Pixel (2053, 1435)

Only the active pixels are used for performance and defect tests.

OverClocking

The test system timing is configured such that the sensor is overclocked in both the vertical and horizontal directions. See Figure 16 for a pictorial representation of the regions.

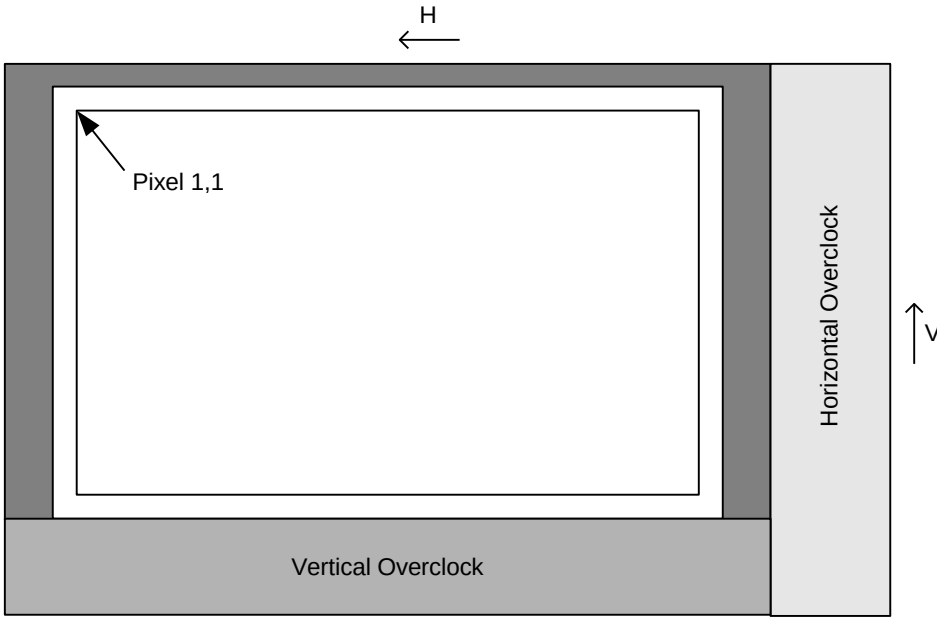


Figure 16: Overclock Regions of Interest

TESTS

Dark Field Defect Test

This test is performed under dark field conditions. The sensor is partitioned into 384 sub regions of interest, each of which is 167 by 167 pixels in size. In each region of interest, the median value of all pixels is found. For each region of interest, a pixel is marked defective if it is greater than or equal to the median value of that region of interest plus the defect threshold specified in the "Defect Definitions" section.

Bright Field Defect Test

This test is performed with the imager illuminated to a level such that the output is at approximately 40,000 electrons. Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 60,000 electrons. The average signal level of all active pixels is found. The bright and dark thresholds are set as:

Dark defect threshold = Active Area Signal * threshold

Bright defect threshold = Active Area Signal * threshold

The sensor is then partitioned into 384 sub regions of interest, each of which is 167 by 167 pixels in size. In each region of interest, the average value of all pixels is found. For each region of interest, a pixel is marked defective if it is greater than or equal to the median value of that region of interest plus the bright threshold specified or if it is less than or equal to the median value of that region of interest minus the dark threshold specified.

Example for major bright field defective pixels:

- Average value of all active pixels is found to be 520 mV (40,000 electrons).
- Dark defect threshold: 520mV * 15% = 78 mV
- Bright defect threshold: 520mV * 15% = 78 mV
- Region of interest #1 selected. This region of interest is pixels 1,1 to pixels 167,167.
    - Median of this region of interest is found to be 520 mV.
    - Any pixel in this region of interest that is ≥ (520+78 mV) 598 mV in intensity will be marked defective.
    - Any pixel in this region of interest that is ≤ (520-78 mV) 442 mV in intensity will be marked defective.
- All remaining 384 sub regions of interest are analyzed for defective pixels in the same manner.

Operation

Maximum Ratings

Absolute maximum rating is defined as a level or condition that should not be exceeded at any time per the description. If the level or the condition is exceeded, the device will be degraded and may be damaged.

Description	Symbol	Minimum	Maximum	Units	Notes
Operating Temperature	T_{OP}	-50	70	°C	1
Humidity	RH	5	90	%	2
Output Bias Current	Iout	0.0	-40	mA	3
Off-chip Load	CL		10	pF	

Notes:
1. Noise performance will degrade at higher temperatures.
2. T=25 °C. Excessive humidity will degrade MTTF.
3. Total for both outputs. Current is -20 mA for each output. Avoid shorting output pins to ground or any low impedance source during operation. Amplifier bandwidth increases at higher current and lower load capacitance at the expense of reduced gain (sensitivity). Operation at these values will reduce MTTF.

Maximum Voltage Ratings Between Pins

Description	Minimum	Maximum	Units	Notes
RL, RR, H1BINL, H1BINR, H2SL, H1SL, H1BL, H2BL, H2BR, H1BR, H1SR, H2SR, OGL, OGR to ESD	0	17	V	
Pin to Pin with ESD Protection	-17	17	V	1
VDDL, VDDR to GND	0	25	V	

Notes:
1. Pins with ESD protection are: RL, RR, H1BINL, H1BINR, H2SL, H1SL, H1BL, H2BL, H2BR, H1BR, H1SR, H2SR, OGL, and OGR.

DC Bias Operating Conditions

Description	Symbol	Minimum	Nominal	Maximum	Units	Maximum DC Current (mA)	Notes
Output Gate	OG	-3.0	-2.5	-2.0	V	1 µA	
Reset Drain	RD	10.5	11.5	12.0	V	1 µA	
Output Amplifier Supply	VDD	14.5	15.0	15.5	V	2 mA	4
Ground	GND	0.0	0.0	0.0	V		
Substrate	SUB	8.0	TBD	17.0	V		1, 5
ESD Protection	ESD	-9.0	-8.0	-7.0	V		2
Output Bias Current	Iout		-5	-10	mA		3

Notes:
1. The operating of the substrate voltage, Vab, will be marked on the shipping container for each device. The value of Vab is set such that the photodiode charge capacity is 60,000 electrons.
2. VESD must be at least 1 V more negative than H1L and H2L during sensor operation AND during camera power turn on.
3. An output load sink must be applied to Vout to activate output amplifier.
4. The maximum DC current is for one output unloaded. This is the maximum current that the first two stages of one output amplifier will draw. This value is with Vout disconnected.
5. Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions*

Power Up Sequence

1. Substrate
2. ESD Protection
3. All other biases and clocks.

AC Operating Conditions

Clock Levels

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
Vertical CCD Clock High	V2H	7.5	8.0	8.5	V	
Vertical CCD Clocks Midlevel	V1M, V2M	-0.2	0.0	0.2	V	
Vertical CCD Clocks Low	V1L, V2L	-9.5	-9.0	-8.5	V	
Horizontal CCD Clocks Amplitude	H1H, H2H	5.8	6.0	6.2	V	
Horizontal CCD Clocks Low	H1L, H2L	-4.2	-4.0	-3.8	V	
Reset Clock High	RH	1.3	1.5	1.7	V	
Reset Clock Low	RL	-3.7	-3.5	-3.3	V	
Electronic Shutter Voltage	Vshutter	39	40	48	V	2
Fast Dump High	FDH	4.5	5.0	5.5	V	
Fast Dump Low	FDL	-9.5	-9.0	-8.5	V	1

Notes:
1. FDL can use the same supply as Vertical CCD Clocks Low if desired.
2. Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions*

Clock Line Capacitances

Clocks	Capacitance	Units	Notes
V1 to GND	108	nF	1
V2 to GND	118	nF	1
V1 to V2	56	nF	
H1S to GND	27	pF	2
H2S to GND	27	pF	2
H1B to GND	13	pF	2
H2B to GND	4	pF	2
H1S to H2B and H2S	13	pF	2
H1B to H2B and H2S	13	pF	2
H2S to H1B and H1S	13	pF	2
H2B to H1B and H1S	13	pF	2
H1BIN to GND	20	pF	2
R to GND	10	pF	
FD to GND	20	pF	

Notes:
1. Gate capacitance to GND is voltage dependent. Value is for nominal VCCD clock voltages.
2. For nominal HCCD clock voltages, these values are for half of the imager (H1SL, H1BL, H2SL, H2BL and H1BINL or H1SR, H1BR, H2SR, H2BR and H1BINR).

TIMING REQUIREMENTS

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
HCCD Delay	T_{HD}	3.0	3.5	10.0	µs	
VCCD Transfer time	T_{VCCD}	3.0	3.5	20.0	µs	
Photodiode Transfer time	T_{V3rd}	8.0	10.0	15.0	µs	
VCCD Pedestal time	T_{3P}	100.0	120.0	200.0	µs	
VCCD Delay	T_{3D}	15.0	20.0	80.0	µs	
Reset Pulse time	T_R	2.5	5.0		ns	
Shutter Pulse time	T_S	3.0	4.0	10.0	µs	
Shutter Pulse delay	T_{SD}	1.0	1.5	10.0	µs	
HCCD Clock Period	T_H	33		200	ns	
VCCD rise/fall time	T_{VR}	0.0	0.1	1.0	µs	
Fast Dump Gate delay	T_{FD}	0.5			µs	
Vertical Clock Edge Alignment	T_{VE}	0.0		100	ns	

MAIN TIMING – CONTINUOUS MODE

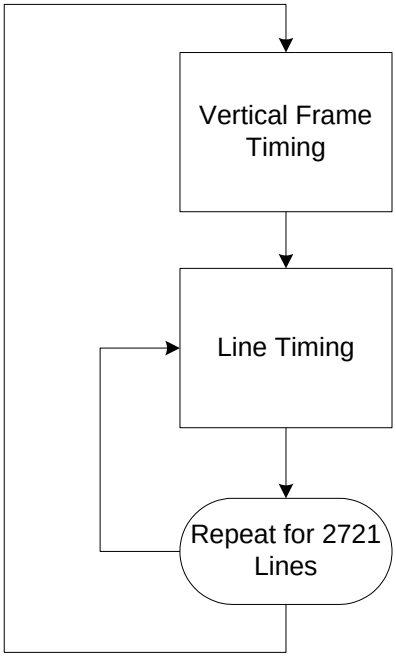


Figure 17: Main Timing - Continuous Mode

FRAME TIMING – CONTINUOUS MODE

Frame Timing without Binning

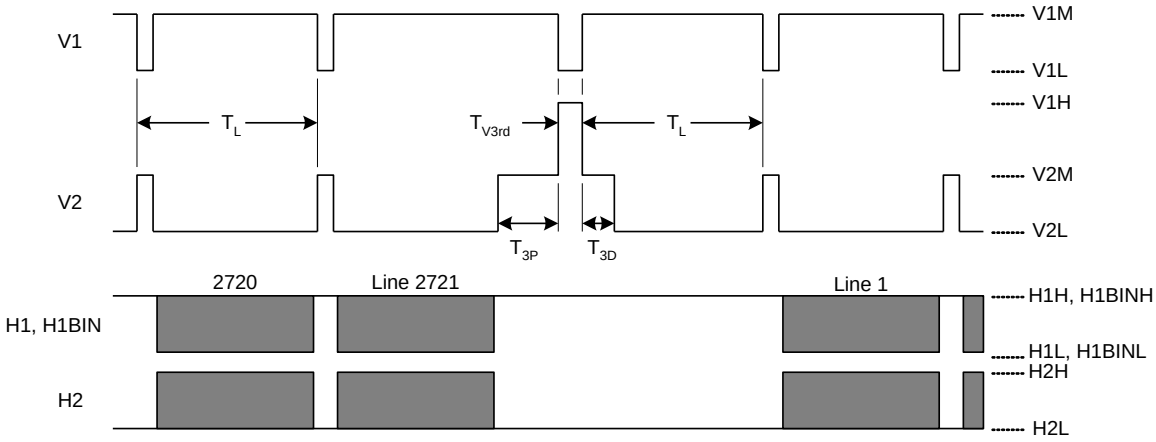


Figure 18: Framing Timing without Binning

Frame Timing for Vertical Binning by 2

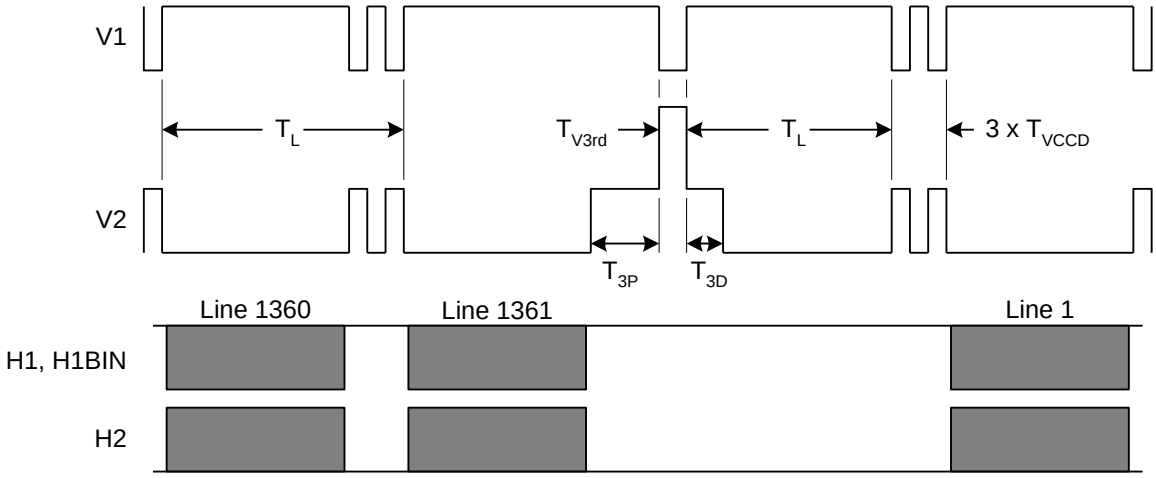


Figure 19: Frame Timing for Vertical Binning by 2

Frame Timing Edge Alignment

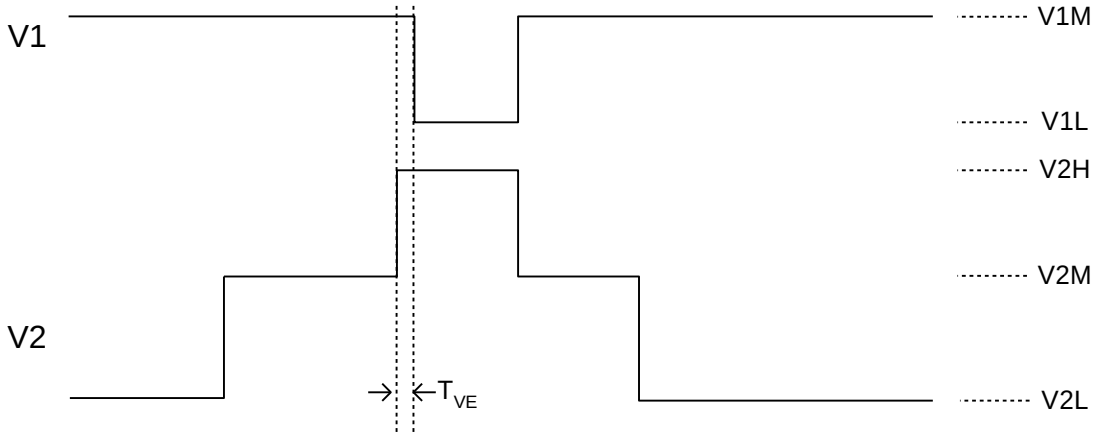


Figure 20: Frame Timing Edge Alignment

LINE TIMING – CONTINUOUS MODE

Line Timing Single Output

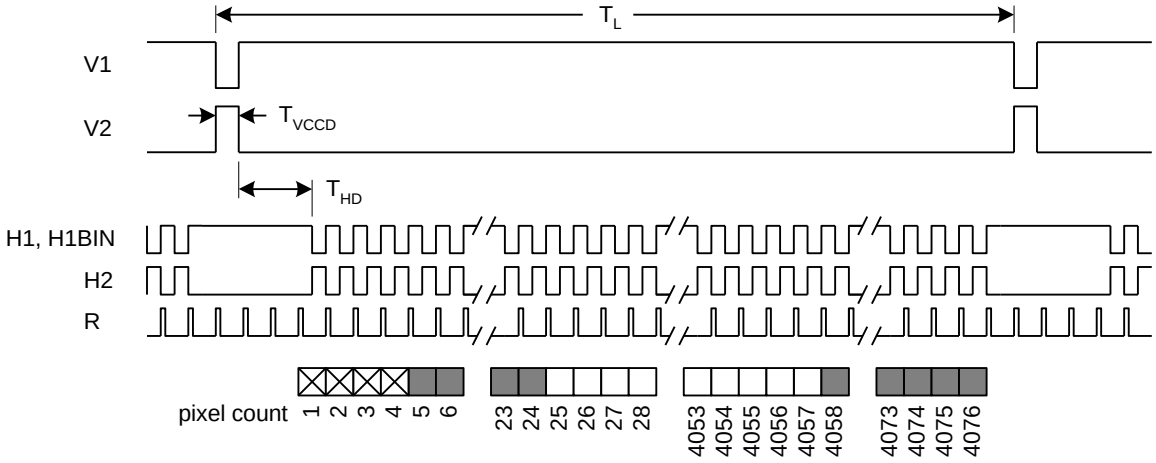


Figure 21: Line Timing Single Output

Line Timing Dual Output – Left Output

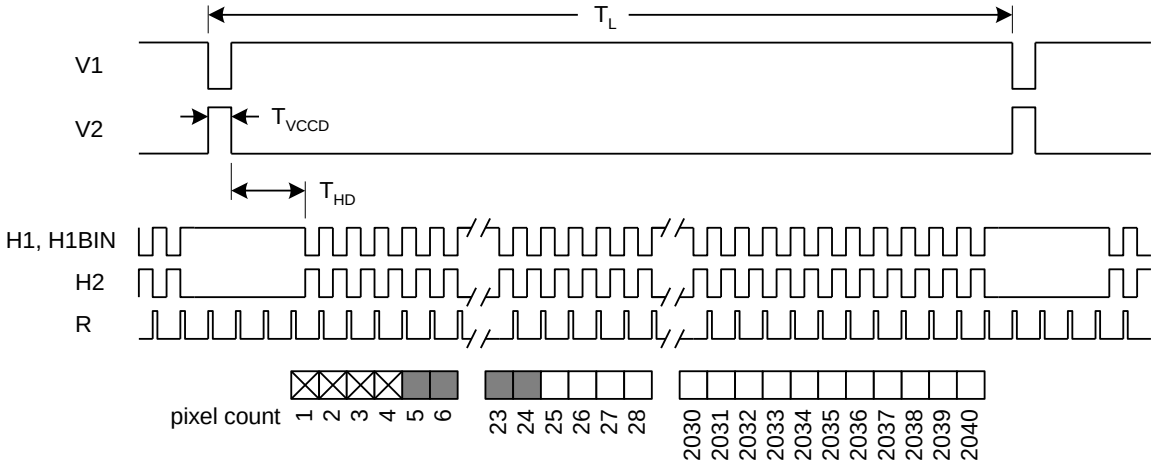


Figure 22: Line Timing Dual Output – Left Output

Line Timing Dual Output – Right Output

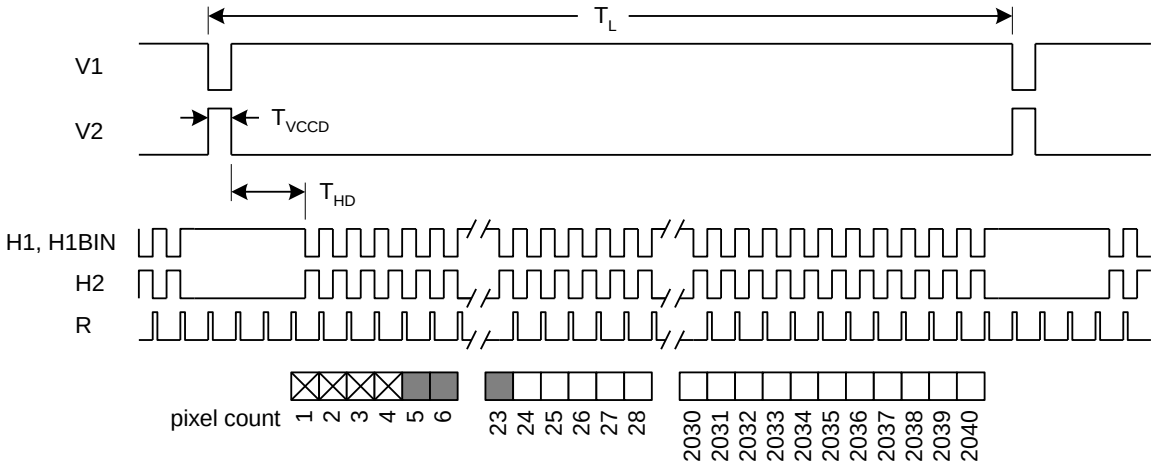


Figure 23: Line Timing Dual Output – Right Output

Line Timing Vertical Binning by 2

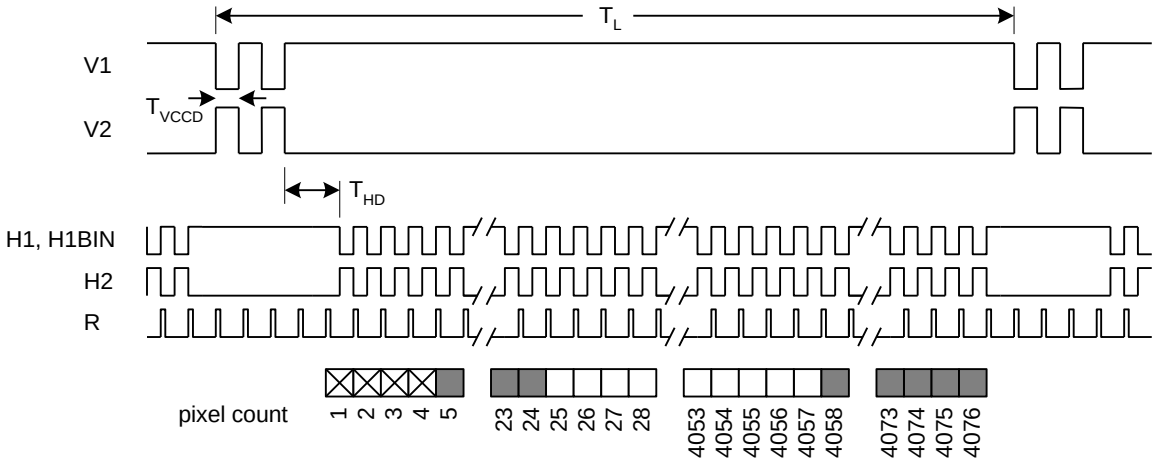


Figure 24: Line Timing Vertical Binning by 2

Line Timing Detail

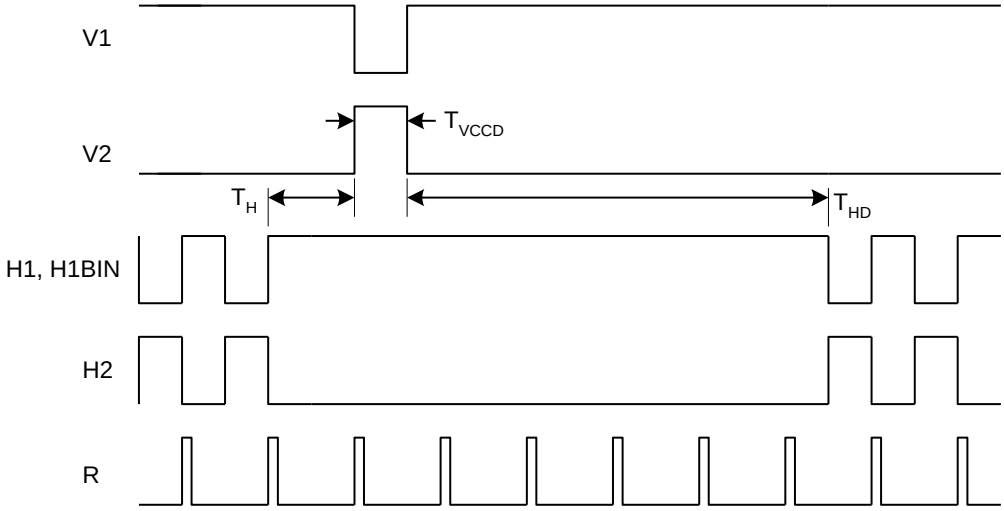


Figure 25: Line Timing Detail

Line Timing Binning by 2 Detail

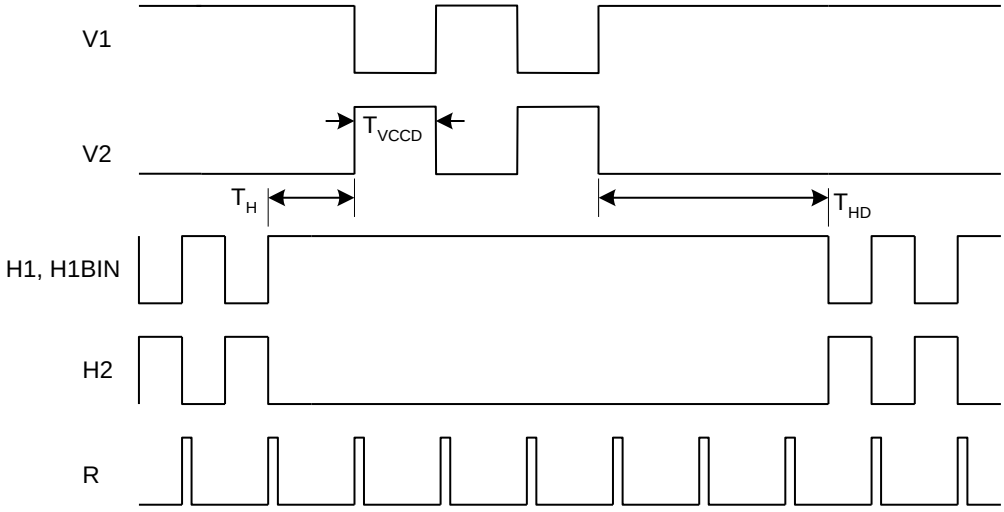


Figure 26: Line Timing by 2 Detail

Line Timing Edge Alignment

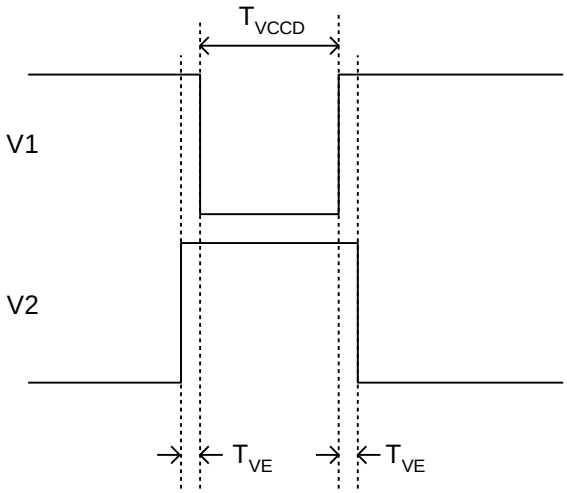


Figure 27: Line Timing Edge Alignment

PIXEL TIMING – CONTINUOUS MODE

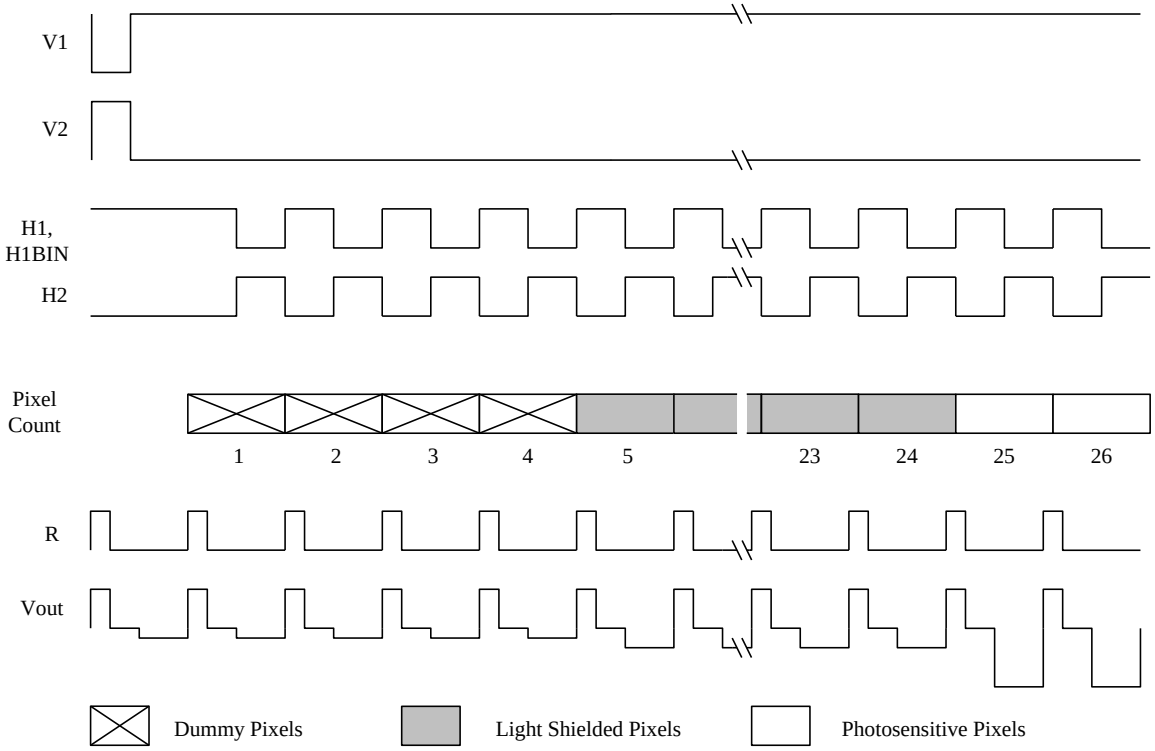


Figure 28: Pixel Timing

Pixel Timing Detail

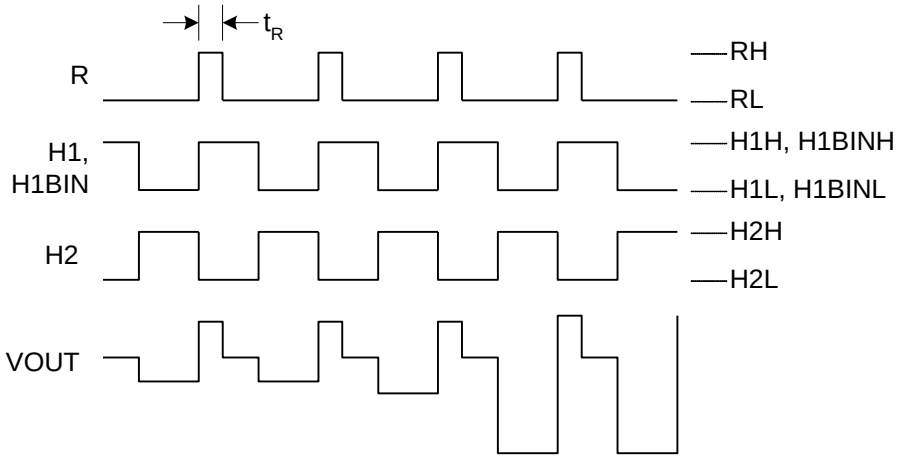


Figure 29: Pixel Timing Detail

FAST LINE DUMP TIMING

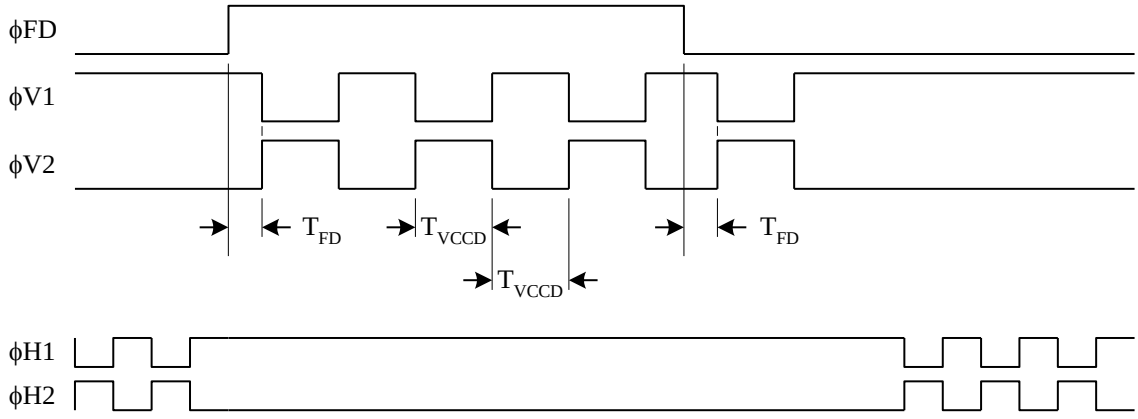


Figure 30: Fast Line Dump Timing

ELECTRONIC SHUTTER

Electronic Shutter Line Timing

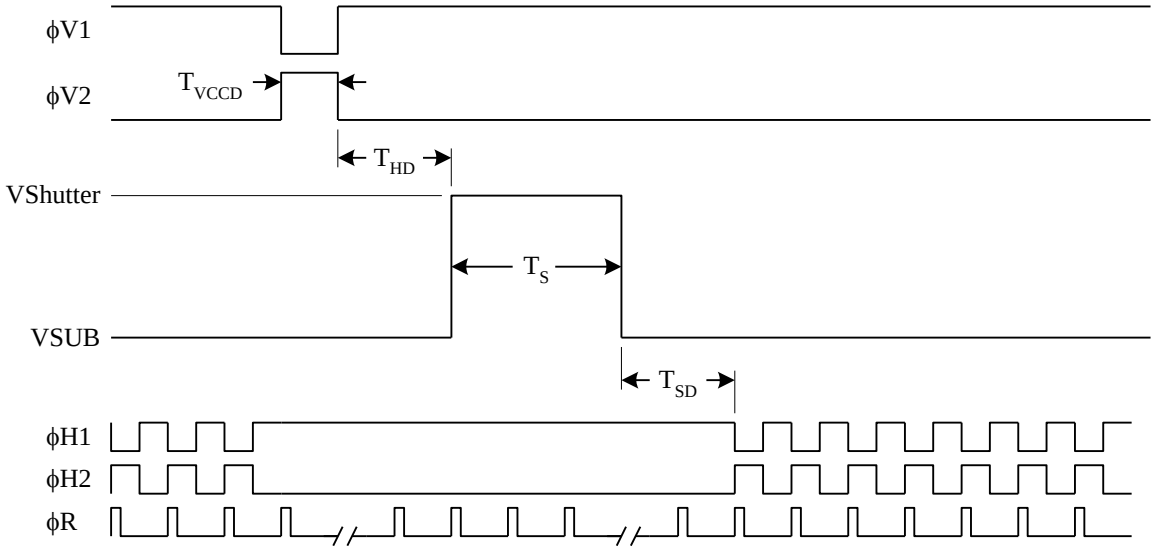


Figure 31: Electronic Shutter Line Timing

Electronic Shutter – Integration Time Definition

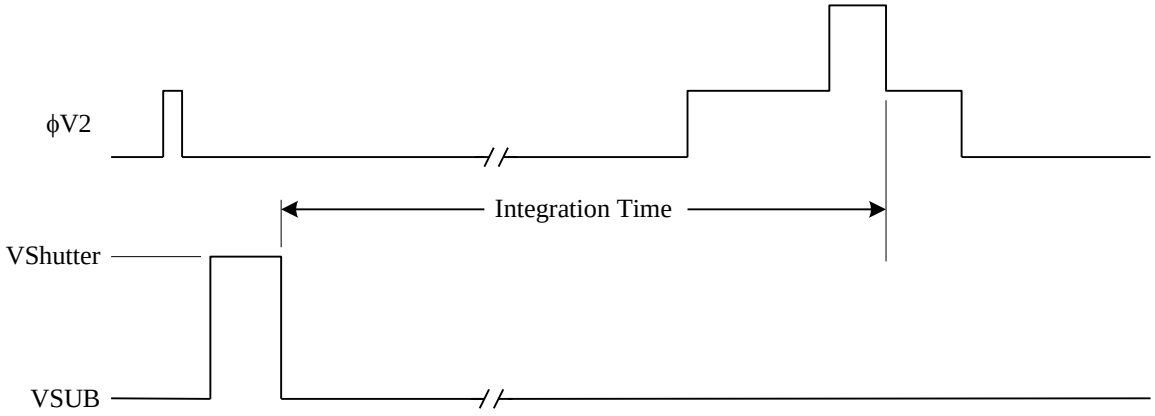


Figure 32: Integration Time Definition

Electronic Shutter Description

The voltage on the substrate (SUB) determines the charge capacity of the photodiodes. When SUB is 8 volts the photodiodes will be at their maximum charge capacity. Increasing VSUB above 8 volts decreases the charge capacity of the photodiodes until 40 volts when the photodiodes have a charge capacity of zero electrons. Therefore, a short pulse on SUB, with a peak amplitude greater than 40 volts, empties all photodiodes and provides the electronic shuttering action.

It may appear the optimal substrate voltage setting is 8 volts to obtain the maximum charge capacity and dynamic range. While setting VSUB to 8 volts will provide the maximum dynamic range, it will also provide the minimum antiblooming protection.

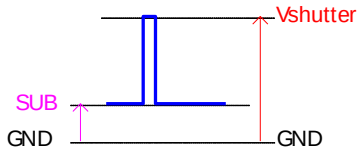
The KAI-11002 VCCD has a charge capacity of 90,000 electrons (90 ke^-). If the SUB voltage is set such that the photodiode holds more than 90 ke^-, then when the charge is transferred from a full photodiode to VCCD, the VCCD will overflow. This overflow condition manifests itself in the image by making bright spots appear elongated in the vertical direction. The size increase of a bright spot is called blooming when the spot doubles in size.

The blooming can be eliminated by increasing the voltage on SUB to lower the charge capacity of the photodiode. This ensures the VCCD charge capacity is greater than the photodiode capacity. There are cases where an extremely bright spot will still cause blooming in the VCCD. Normally, when the photodiode is full, any additional electrons generated by photons will spill out of the photodiode. The excess electrons are drained harmlessly out to the substrate. There is a maximum rate at which the electrons can be drained to the substrate. If that maximum rate is exceeded, (for example, by a very bright light source) then it is possible for the total amount of charge in the photodiode to exceed the VCCD capacity. This results in blooming.

The amount of antiblooming protection also decreases when the integration time is decreased. There is a compromise between photodiode dynamic range (controlled by VSUB) and the amount of antiblooming protection. A low VSUB voltage provides the maximum dynamic range and minimum (or no) antiblooming protection. A high VSUB voltage provides lower dynamic range and maximum antiblooming protection. The optimal setting of VSUB is written on the container in which each KAI-11002 is shipped. The given VSUB voltage for each sensor is selected to provide antiblooming protection for bright spots at least 100 times saturation, while maintaining at least 60 ke- of dynamic range.

The electronic shutter provides a method of precisely controlling the image exposure time without any mechanical components. If an integration time of TINT is desired, then the substrate voltage of the sensor is pulsed to at least 40 volts TINT seconds before the photodiode to VCCD transfer pulse on V2. Use of the electronic shutter does not have to wait until the previously acquired image has been completely read out of the VCCD.

The figure below shows the DC bias (SUB) and AC clock (Vshutter) applied to the SUB pin. Both the DC bias and AC clock are referenced to ground.



Storage and Handling

Storage Conditions

Description	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	T_{ST}	-20	80	°C	1
Humidity	RH	5	90	%	2

Notes:
1. Long-term exposure toward the maximum temperature will accelerate color filter degradation.
2. T=25 °C. Excessive humidity will degrade MTTF

ESD

1. This device contains limited protection against Electrostatic Discharge (ESD). ESD events may cause irreparable damage to a CCD image sensor either immediately or well after the ESD event occurred. Failure to protect the sensor from electrostatic discharge may affect device performance and reliability.
2. Devices should be handled in accordance with strict ESD procedures for Class 0 (<250V per JESD22 Human Body Model test), or Class A (<200V JESD22 Machine Model test) devices. Devices are shipped in static-safe containers and should only be handled at static-safe workstations.
3. See Application Note *Image Sensor Handling Best Practices* for proper handling and grounding procedures. This application note also contains workplace recommendations to minimize electrostatic discharge.
4. Store devices in containers made of electro-conductive materials.

Cover Glass Care and Cleanliness

1. The cover glass is highly susceptible to particles and other contamination. Perform all assembly operations in a clean environment.
2. Touching the cover glass must be avoided.
3. Improper cleaning of the cover glass may damage these devices. Refer to Application Note *Image Sensor Handling Best Practices*.

Environmental Exposure

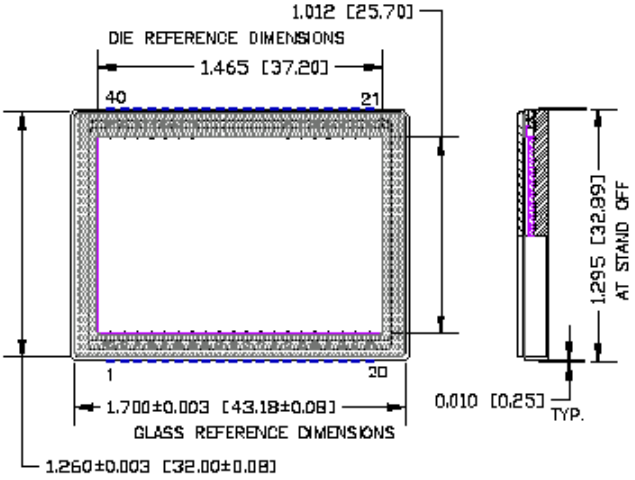
1. Extremely bright light can potentially harm CCD image sensors. Do not expose to strong sunlight for long periods of time, as the color filters and/or microlenses may become discolored. In addition, long time exposures to a static high contrast scene should be avoided. Localized changes in response may occur from color filter/microlens aging. For Interline devices, refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible lighting Conditions*.
2. Exposure to temperatures exceeding maximum specified levels should be avoided for storage and operation, as device performance and reliability may be affected.
3. Avoid sudden temperature changes.
4. Exposure to excessive humidity may affect device characteristics and may alter device performance and reliability, and therefore should be avoided.
5. Avoid storage of the product in the presence of dust or corrosive agents or gases, as deterioration of lead solderability may occur. It is advised that the solderability of the device leads be assessed after an extended period of storage, over one year.

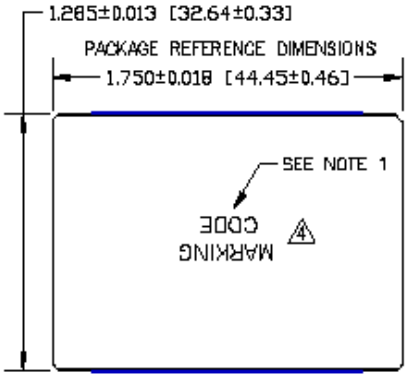
Soldering Recommendations

1. The soldering iron tip temperature is not to exceed 370 °C. Higher temperatures may alter device performance and reliability.
2. Flow soldering method is not recommended. Solder dipping can cause damage to the glass and harm the imaging capability of the device. Recommended method is by partial heating using a grounded 30W soldering iron. Heat each pin for less than 2 seconds duration.

Mechanical Information

PACKAGE





NOTES:
1. SEE ORDERING INFORMATION FOR MARKING CODE
2. COVER GLASS IS MANUALLY PLACED AND VISUALLY ALIGNED OVER DIE – LOCATION ACCURACY IS NOT GUARANTEED.

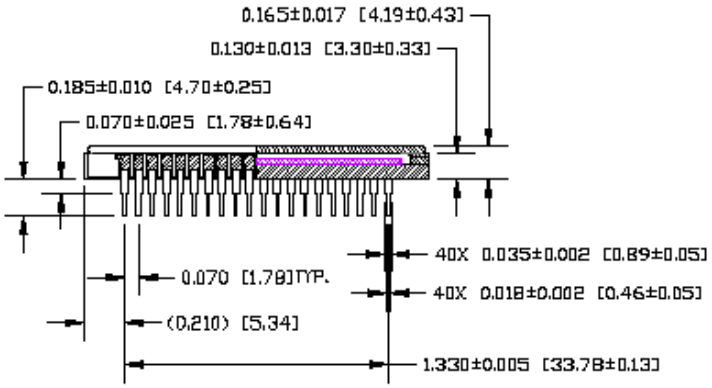


Figure 33: Package Drawing

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DIE TO PACKAGE ALIGNMENT

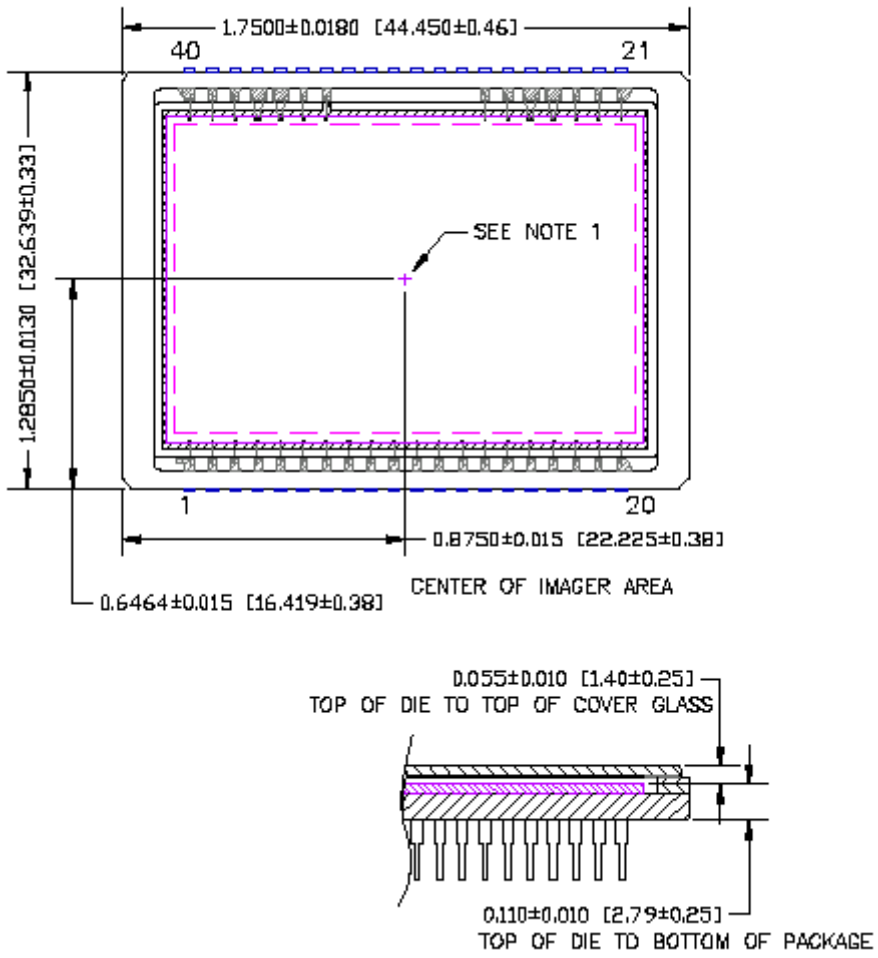
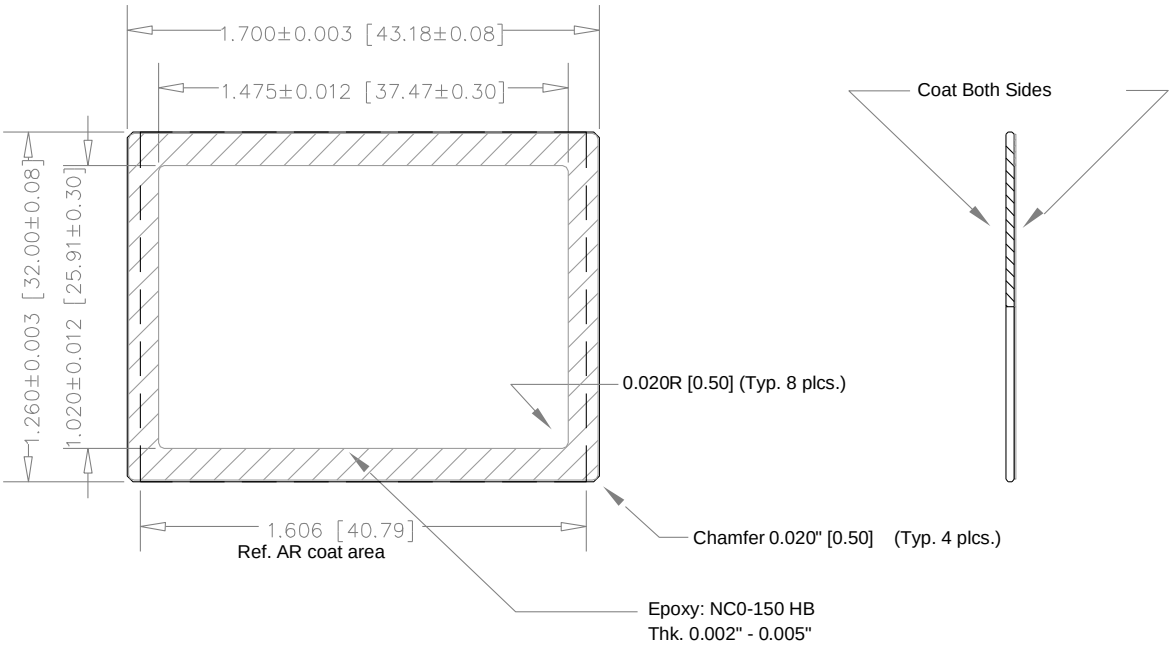
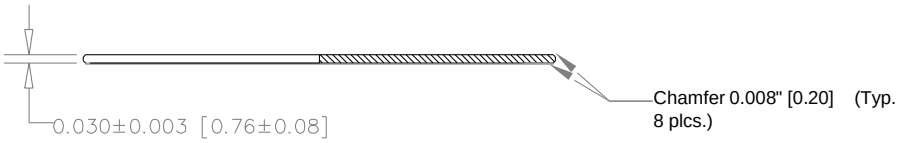


Figure 34: Die to Package Alignment

Glass





NOTES:

1. Multi-Layer Anti-Reflective Coating on 2 sides:
   Double Sided Reflectance:
   Range (nm)
   420 - 450 nm < 2%
   450 - 630 nm < 1%
   630 - 680 nm < 2%
2. Dust, Scratch specification - 20 microns max.
3. Substrate - Schott D263T eco or Equivalent
4. Epoxy: NCO-150HB
   Thickness: 0.002" - 0.005"

Figure 35: Glass Drawing

GLASS TRANSMISSION

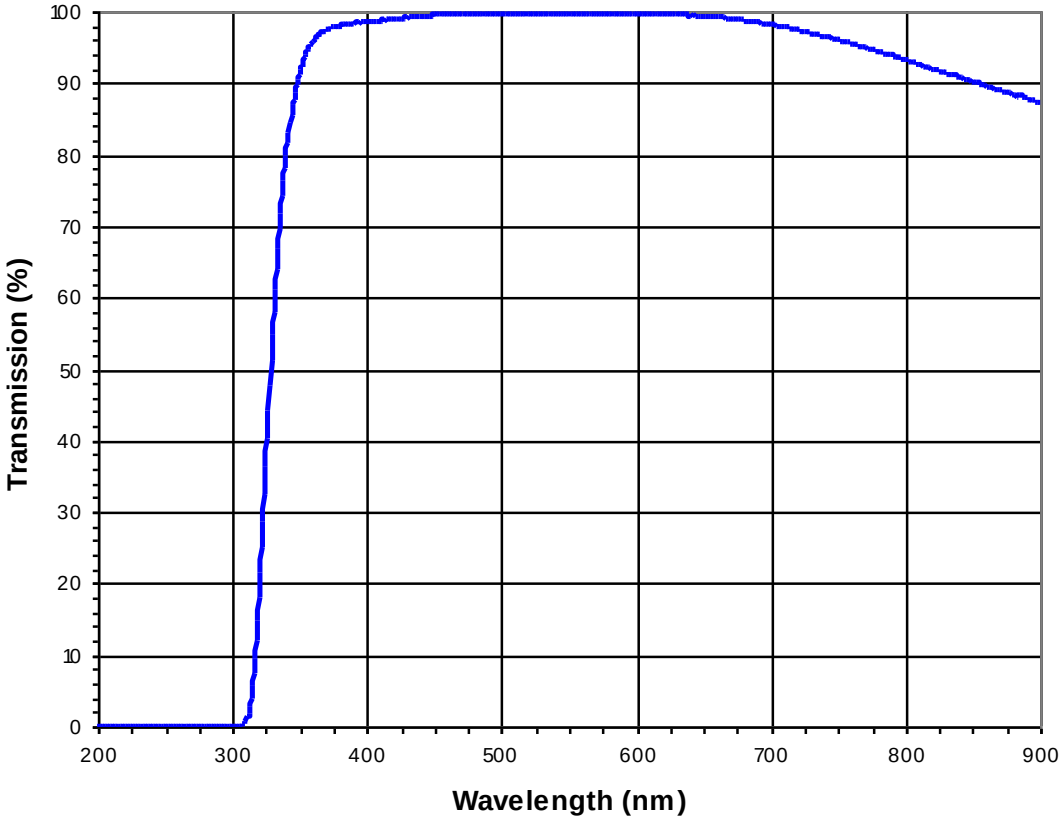


Figure 36: Glass Transmission

Quality Assurance and Reliability

Quality and Reliability

All image sensors conform to the specifications stated in this document. This is accomplished through a combination of statistical process control and visual inspection and electrical testing at key points of the manufacturing process, using industry standard methods. Information concerning the quality assurance and reliability testing procedures and results are available from ON Semiconductor upon request. For further information refer to Application Note *Quality and Reliability*.

Replacement

All devices are warranted against failure in accordance with the *Terms of Sale*. Devices that fail due to mechanical and electrical damage caused by the customer will not be replaced.

Liability of the Supplier

A reject is defined as an image sensor that does not meet all of the specifications in this document upon receipt by the customer. Product liability is limited to the cost of the defective item, as defined in the *Terms of Sale*.

Liability of the Customer

Damage from mishandling (scratches or breakage), electrostatic discharge (ESD), or other electrical misuse of the device beyond the stated operating or storage limits, which occurred after receipt of the sensor by the customer, shall be the responsibility of the customer.

Test Data Retention

Image sensors shall have an identifying number traceable to a test data file. Test data shall be kept for a period of 2 years after date of delivery.

Mechanical

The device assembly drawing is provided as a reference.

ON Semiconductor reserves the right to change any information contained herein without notice. All information furnished by ON Semiconductor is believed to be accurate.

Life Support Applications Policy

ON Semiconductor image sensors are not authorized for and should not be used within Life Support Systems without the specific written consent of ON Semiconductor.

Revision Changes

MTD/PS-0938

Revision Number	Description of Changes
1.0	• Initial formal release
2.0	• Reformatted Ordering Information, Storage and Handling, and Quality Assurance and Reliability pages
3.0	• Added the note "Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions*" to the following sections ○ DC Bias Operating Conditions ○ AC Operating Conditions ○ Storage and Handling • Added figure in Electronic Shutter Description section showing relationship between ground and the substrate DC bias and the electronic shutter pulse • Changed cover glass material to D263T eco or equivalent

PS-0012

Revision Number	Description of Changes
1.0	• Initial release with new document number, updated branding and document template • Updated *Storage and Handling* and *Quality Assurance and Reliability* sections • Reorganized structure for consistency with other Interline Transfer CCD documents
1.1	• Updated branding

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