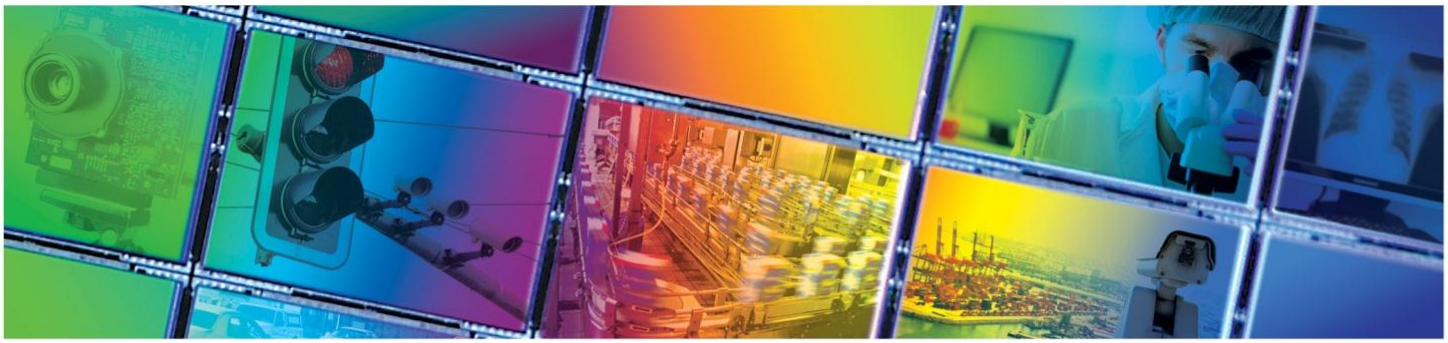
ON Semiconductor®

KAI-1020 IMAGE SENSOR

1000 (H) X 1000 (V) INTERLINE CCD IMAGE SENSOR



JUNE 9, 2014

DEVICE PERFORMANCE SPECIFICATION

REVISION 2.1 PS-0019

TABLE OF CONTENTS

TABLE OF FIGURES

Summary Specification

KAI-1020 Image Sensor

DESCRIPTION

The KAI-1020 Image Sensor is a one megapixel interline CCD with integrated clock drivers and on-chip correlated double sampling. The progressive scan architecture and global electronic shutter provide excellent image quality for full motion video and still image capture.

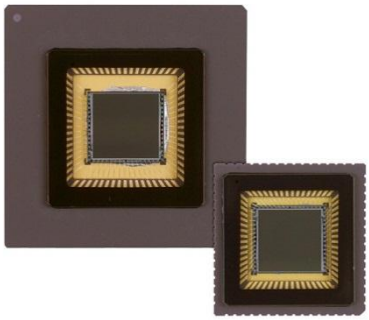
The integrated clock drivers allow for easy integration with CMOS logic timing generators. The sensor features a fast line dump for high-speed sub-window readout and single (30 fps) or dual (48 fps) output operation.

FEATURES

- 10 bits dynamic range at 40 MHz
- Large 7.4 µm square pixels for high sensitivity
- Progressive scan (non-interlaced)
- Integrated vertical clock drivers
- Integrated correlated double sampling (CDS) up to 40 MHz
- Integrated electronic shutter driver
- Reversible HCCD capable of 40MHz operation All timing inputs 0 to 5 Volts
- Single or dual video output operation
- Progressive scan or interlaced
- Fast dump gate for high speed sub-window readout
- Antiblooming protection

APPLICATIONS

- Machine Vision
- Medical
- Scientific
- Surveillance



Parameter	Typical Value
Architecture	Interline CCD, Progressive Scan
Total Number of Pixels	1028 (H) x 1008 (V)
Number of Effective Pixels	1004 (H) x 1004 (V)
Number of Active Pixels	1000 (H) x 1000 (V)
Pixel Size	7.4 µm (H) x 7.4 µm (V)
Active Image Size	7.4 mm (H) x 7.4 mm (V) 10.5 mm (diagonal)
Aspect Ratio	1:1
Number of Outputs	1 or 2
Saturation Signal	40,000 electrons
Output Sensitivity	12 µV/electron
Quantum Efficiency -ABA (500nm) -CBA (620 nm, 540 nm, 460nm)	 44% 31%, 36%, 41%
Dark Noise	50 electrons rms
Dark Current (Typical)	<0.5 nA/cm^2
Dynamic Range	58 dB
Blooming Suppression	100 X
Image Lag	<10 electrons
Smear	<0.03%
Maximum Data Rate	40 MHz/Channel (2 channels)
Frame Rate Progressive Scan, One Output Progressive Scan, Dual Outputs Interlaced Scan, One Output	 30 fps 48 fps 49 fps
Integrated Vertical Clock Drivers	
Integrated Correlated Double Sampling (CDS)	
Integrated Electronic Shutter Driver	
Package	68 pin PGA or 64 pin CLCC
Cover Glass	AR coated, 2 sides

All parameters above are specified at T = 40 °C

Ordering Information

Catalog Number	Product Name	Description	Marking Code
2H4889	KAI- 1020-AAA-JP-BA	Monochrome, No Microlens, PGA Package, Taped Clear Cover Glass, no coatings, Standard Grade	KAI-1020 Serial Number
4H0934	KAI- 1020-ABB-FD-AE	Monochrome, Telecentric Microlens, CLCC Package, Clear Cover Glass with AR coating (both sides), Engineering Sample	KAI-1020-ABB Serial Number
4H0933	KAI- 1020-ABB-FD-BA	Monochrome, Telecentric Microlens, CLCC Package, Clear Cover Glass with AR coating (both sides), Standard Grade	
4H2319	KAI- 1020-ABB-JP-AE	Monochrome, Telecentric Microlens, PGA Package, Taped Clear Cover Glass (no coatings), Engineering Sample	
4H2318	KAI- 1020-ABB-JP-BA	Monochrome, Telecentric Microlens, PGA Package, Taped Clear Cover Glass (no coatings), Standard Grade	
4H0932	KAI- 1020-ABB-JB-AE	Monochrome, Telecentric Microlens, PGA Package, Clear Cover Glass (no coatings), Engineering Sample	
4H0931	KAI- 1020-ABB-JB-BA	Monochrome, Telecentric Microlens, PGA Package, Clear Cover Glass (no coatings), Standard Grade	
4H0910	KAI- 1020-ABB-JD-AE	Monochrome, Telecentric Microlens, PGA Package, Clear Cover Glass with AR coating (both sides), Engineering Sample	
4H0935	KAI- 1020-ABB-JD-BA	Monochrome, Telecentric Microlens, PGA Package, Clear Cover Glass with AR coating (both sides), Standard Grade	
2H4996	KAI- 1020-CBA-FD-AE	Color (Bayer RGB), Telecentric Microlens, CLCC Package, Clear Cover Glass with AR coating (both sides), Engineering Sample	KAI-1020CM Serial Number
4H0131	KAI- 1020-CBA-FD-BA	Color (Bayer RGB), Telecentric Microlens, CLCC Package, Clear Cover Glass with AR coating (both sides), Standard Grade	
4H0194	KAI- 1020-CBA-JD-AE	Color (Bayer RGB), Telecentric Microlens, PGA Package, Clear Cover Glass with AR coating (both sides), Engineering Sample	
4H0193	KAI- 1020-CBA-JD-BA	Color (Bayer RGB), Telecentric Microlens, PGA Package, Clear Cover Glass with AR coating (both sides), Standard Grade	
1E9790	KEK-1E9790-KAI-1020-12-40	Evaluation Board (Complete Kit)	n/a

See Application Note *Product Naming Convention* for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.truesenseimaging.com.

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Device Description

ARCHITECTURE

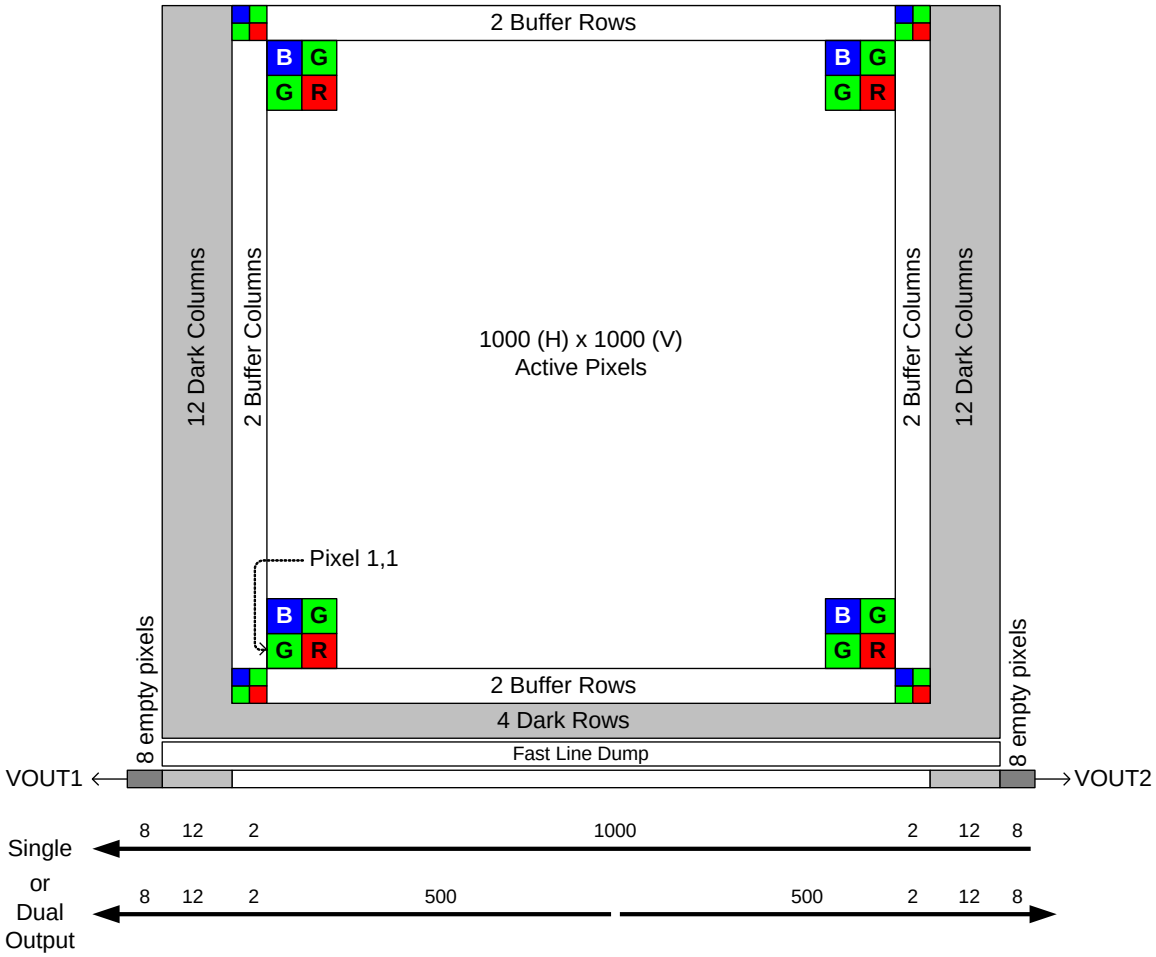


Figure 1: Block Diagram

There are 4 light shielded rows followed 1004 photoactive rows. The first 2 and the last 2 photoactive rows are buffer rows giving a total of 1000 lines of image data.

In the single output mode all pixels are clocked out of the Video 1 output in the lower left corner of the sensor. The first 8 empty pixels of each line do not receive charge from the vertical shift register. The next 12 pixels receive charge from the left light-shielded edge followed by 1004 photo-sensitive pixels and finally 12 more light shielded pixels from the right edge of the sensor. The first and last 2 photosensitive pixels are buffer pixels giving a total of 1000 pixels of image data.

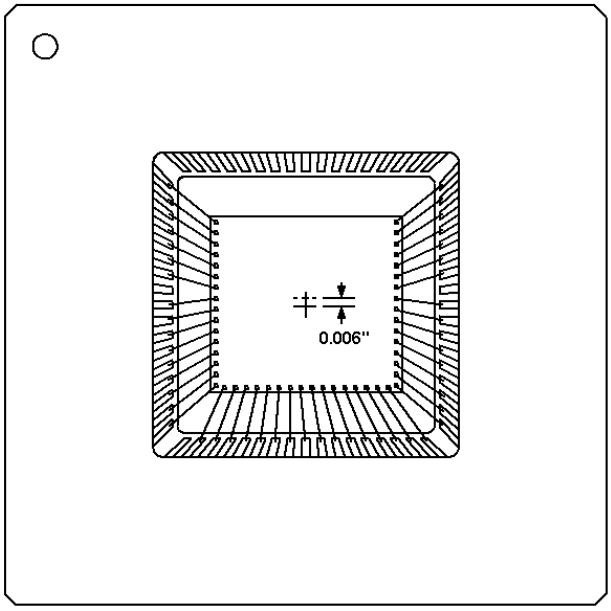
In the dual output mode the clocking of the right half of the horizontal CCD is reversed. The left half of the image is clocked out Video 1 and the right half of the image is clocked out Video 2. Each row consists of 8 empty pixels followed by 12 light shielded pixels followed by 502 photosensitive pixels. When reconstructing the image, data from Video 2 will have to be reversed in a line buffer and appended to the Video 1 data.

PHYSICAL DESCRIPTION

Pin Description and Device Orientation

Pin Grid Array

When viewed from the top with the pin 1 index to the upper left, the center of the photoactive pixel array is offset 0.006" above the physical center of the package. The pin 1 index is located in the corner of the package above pins L2 and K1. When operated in single output mode the first pixel out of the sensor will be in the corner closest to VOUT1B (pin L9). The HCCD is parallel to the row of pins A10 to L10. In the pictures below, the VCCD transfers charge down.



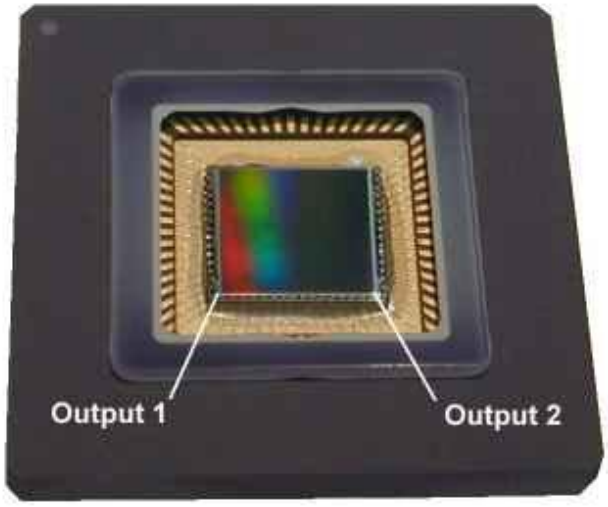


Figure 2: Pin 1 Location

Pin Grid Array Pin Description

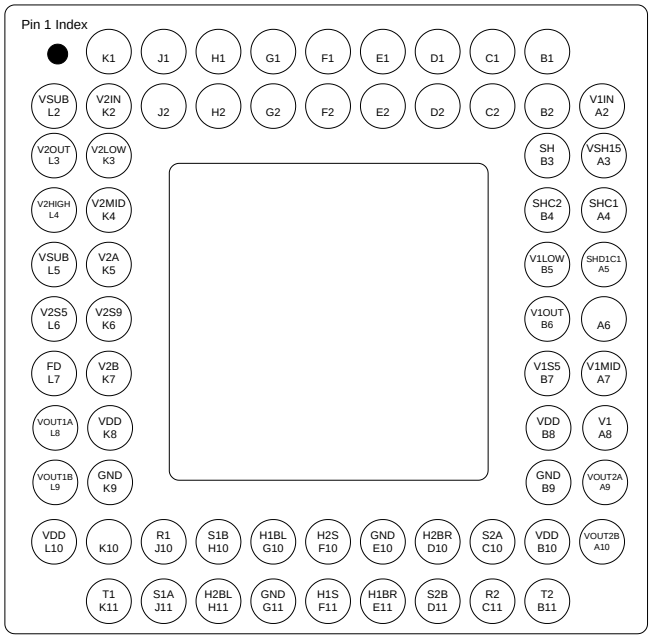


Figure 3: PGA Package Pin Designations - Top View

Label	Pin	Function
V2IN	K2	VCCD gate phase 2 input
VSUB	L2	substrate voltage input
V2LOW	K3	VCCD phase 2 clock driver low
V2OUT	L3	VCCD phase 2 clock driver output
V2MID	K4	VCCD phase 2 clock driver mid
V2HIGH	L4	VCCD phase 2 clock driver high
V2A	K5	VCCD phase 2 clock driver input A
VSUB	L5	substrate voltage input
V2S9	K6	VCCD phase 2 clock driver +9V
V2S5	L6	VCCD phase 2 clock driver +5V fast dump clock driver +5V
φV2B	K7	VCCD phase 2 clock driver input B
φFD	L7	fast dump clock driver input
VDD1	K8	Video 1 CDS +15V
VOUT1A	L8	Video 1 CDS output A
GND	K9	Ground (0V)
VOUT1B	L9	Video 1 CDS output B
VDD1	L10	Video 1 CDS +15V supply
φT1	K11	Video 1 CDS transfer clock input
φR1	J10	Video 1 CDS reset clock input
φS1A	J11	Video 1 CDS sample A clock input
φS1B	H10	Video 1 CDS sample B clock input
φH2BL	H11	HCCD left phase 2 barrier clock input
φH1BL	G10	HCCD left phase 1 barrier clock input
GND	G11	Ground (0V)
φH2S	F10	HCCD storage phase 2 clock input

Label	Pin	Function
φH1S	F11	HCCD storage phase 1 clock input
GND	E10	Ground (0V)
φH1BR	E11	HCCD right phase 1 barrier clock input
φH2BR	D10	HCCD right phase 2 barrier clock input
φS2B	D11	Video 2 CDS sample B clock input
φS2A	C10	Video 2 CDS sample A clock input
φR2	C11	Video 2 CDS reset clock input
φT2	B11	Video 2 CDS transfer clock input
VDD2	B10	Video 2 CDS +15V
VOUT2B	A10	Video 2 CDS output B
GND	B9	Ground (0V)
VOUT2A	A9	Video 2 CDS output A
VDD2	B8	Video 2 CDS +15V
φV1	A8	VCCD phase 1 clock driver input
V1S5	B7	VCCD phase 1 clock driver +5V
V1MID	A7	VCCD phase 1 clock driver mid
V1OUT	B6	VCCD phase 1 clock driver output
V1LOW	B5	VCCD phase 1 clock driver low
SHD1C1	A5	shutter driver connection
SHC2	B4	shutter driver connection
SHC1	A4	shutter driver connection
φSH	B3	shutter driver clock input
VSH15	A3	shutter driver +15V
V1IN	A2	VCCD gate phase 1 input

All pins not listed must be unconnected.

Leadless Chip Carrier

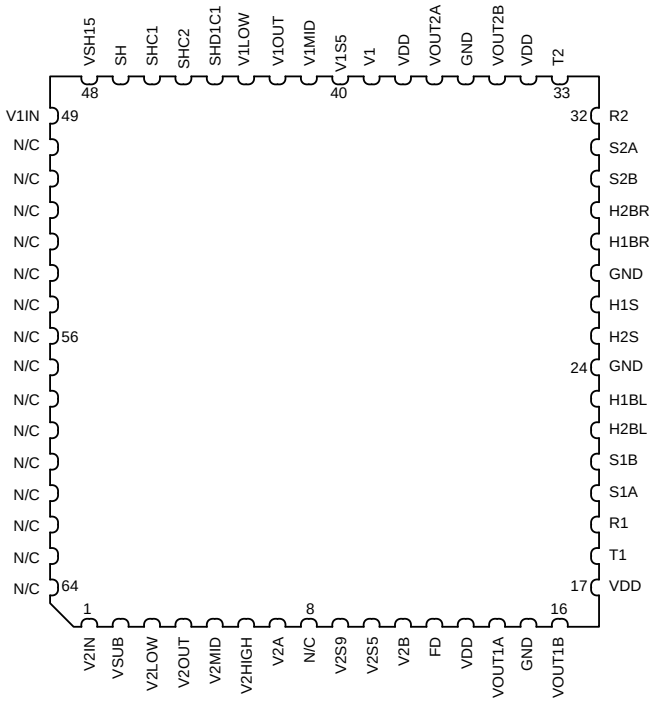


Figure 4: LCC Package Pin Designations - Top View

Pin	Description
1	V2IN
2	VSUB
3	V2LOW
4	V2OUT
5	V2MID
6	V2HIGH
7	V2A
8	No Connect
9	V2S9
10	V2S5
11	V2B
12	FD
13	VDD
14	VOUT1A
15	GND
16	VOUT1B
17	VDD
18	T1
19	R1
20	S1A
21	S1B
22	H2BL
23	H1BL
24	GND
50-64	No Connect

Pin	Description
25	H2S
26	H1S
27	GND
28	H1BR
29	H2BR
30	S2B
31	S2A
32	R2
33	T2
34	VDD
35	VOUT2B
36	GND
37	VOUT2A
38	VDD
39	V1
40	V1S5
41	V1MID
42	V1OUT
43	V1LOW
44	SHD1C1
45	SHC2
46	SHC1
47	SH
48	VSH15
49	V1IN

Imaging Performance

Optical Specification

Symbol	Description	Min.	Nom.	Max.	Units	Notes	Sampling Plan
QE_{max}	Peak Quantum Efficiency	42	45		%	1	Design
λQE	Peak Quantum Efficiency Wavelength		490		nm	1	Design
ΘQE*h*	Microlens Acceptance Angle (horizontal)	±12	±13		degrees	2	Design
ΘQE*v*	Microlens Acceptance Angle (vertical)	±25	±30		degrees	2	Design
QE(540)	Quantum Efficiency at 540nm	38	40		%	1	Design
PNU	Photoresponse nonuniformity		5		%		Design
NL	Maximum Photoresponse Nonlinearity		2		%	3, 4,18	Die
ΔG	Maximum Gain Difference Between Outputs		10		%	3, 4,18	Die
ΔNL	Maximum Signal Error caused by Nonlinearity Differences		1		%	3, 4,18	Die
	Dark Center Uniformity			12	e^- rms	19, 20	Die
	Dark Global Uniformity			2	mVpp	19, 20	Die
	Global Uniformity			5	%rms	19, 20	Die
	Global Peak to Peak Uniformity			15	%pp	19, 20	Die
	Center Uniformity			0.7	%rms	19, 20	Die

CCD Specifications

Symbol	Description	Min.	Nom.	Max.	Units	Notes	Sampling Plan
Vne	Vertical CCD Charge Capacity	54	60		ke^-		Design
Hne	Horizontal CCD Charge Capacity	110	120		ke^-		Design
Pne	Photodiode Charge Capacity	38	42		ke^-	5	Die
Id	Dark Current		0.2	0.5	nA/cm^2	6	Die
Lag	Image Lag		< 10	50	e^-	7	Design
Xab	Antiblooming factor	100	300			1, 8, 9, 10, 11	Design
Smr	Vertical Smear		-75	-72	dB	1, 8, 9	Design

CDS Output Specification

Symbol	Description	Nominal	Units	Notes	Sampling Plan
P_d	Power Dissipation	213	mW	12	Design
F_{-3dB}	Bandwidth	140	MHz	12	Design
C_L	Max Off-chip Load	10	pF	13	Design
A_v	Gain	0.70		12	Design
ΔV/ΔN	Sensitivity	13	$μV/e^-$	12	Design
R	Output Impedance	160	Ω	12	Design
Vsat	Saturation Voltage	500	mV	5, 12	Die
Iout	Output Bias Current	3.0	mA		Design

General – Monochrome

Symbol	Description	Nominal	Units	Notes	Sampling Plan
n_{e-T}	Total Camera Noise	42	e^- rms	6, 14	Design
DR	Dynamic Range	60	dB	15	Design

General Color

Symbol	Description	Nominal	Units	Notes	Sampling Plan
n_{e-T}	Total Camera Noise	50	e- rms	6, 14	Design
DR	Dynamic Range	58	dB	15	Design

Power

Description	Nominal	Units	Notes
Single Channel CDS	213	mW	12
VCCD clock driver	71	mW	16
Electronic shutter driver	1.1	mW	
HCCD	122	mW	16, 17
Total Power	407	mW	12, 16

Notes:

1. Measured with F/4 imaging optics.
2. Value is the angular range of incident light for which the quantum efficiency is at least 50% of QEmax at a wavelength of λQE. Angles are measured with respect to the sensor surface normal in a plane parallel to the horizontal axis (ΘQEh) or in a plane parallel to the vertical axis (ΘQEv).
3. Value is over the range of 10% to 90% of photodiode saturation.
4. Value is for the sensor operated without binning.
5. This value depends on the substrate voltage setting. Higher photodiode saturation charge capacities will lower the antiblooming specification. Substrate voltage will be specified with each part for 42 ke^-.
6. Measured at 40 °C, 40 MHz HCCD frequency.
7. This is the first field decay lag at 70% saturation. Measured by strobe illumination of the device at 70% of photodiode saturation, and then measuring the subsequent frame's average pixel output in the dark.
8. Measured with a spot size of 100 vertical pixels, no electronic shutter.
9. Measured with green light (500 nm to 580 nm).
10. A blooming condition is defined as when the spot size doubles in size.
11. Antiblooming factor is the light intensity which causes blooming divided by the light intensity which first saturates the photodiodes.
12. Single output power, 3 mA load
13. With total output load capacitance of C_L= 10 pF between the outputs and AC ground.
14. Includes system electronics noise, dark pattern noise and dark current shot noise at 40 MHz. Total noise measured on the KAI-1020 evaluation board.
15. Uses 20LOG(Pne/n_{e-T})
16. At 30 frames/sec, single output
17. This includes the power of the external HCCD clock driver.
18. For the sampling plan, measured at 10 MHz
19. Tested at 27 °C and 40 °C
20. See Tests

Sampling plan defined as "die" indicates that every device is verified against the specified performance limits. Sampling plan defined as "design" indicates a sampled test or characterization, at the discretion of Truesense Imaging, against the specified performance limits.

Typical Performance Curves

Monochrome Quantum Efficiency

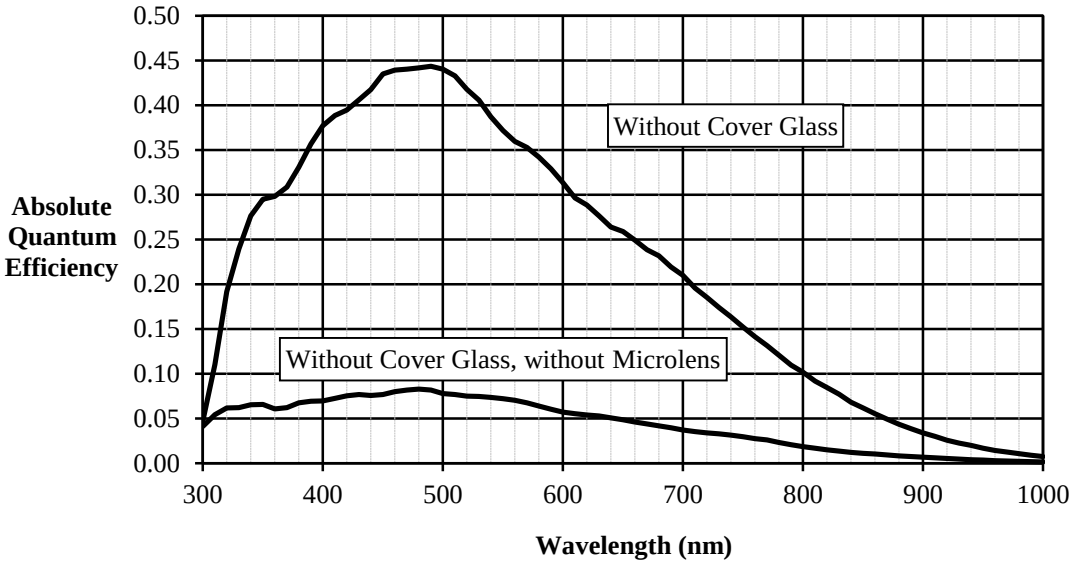


Figure 5: Monochrome Quantum Efficiency

Color (Bayer RGB) Quantum Efficiency

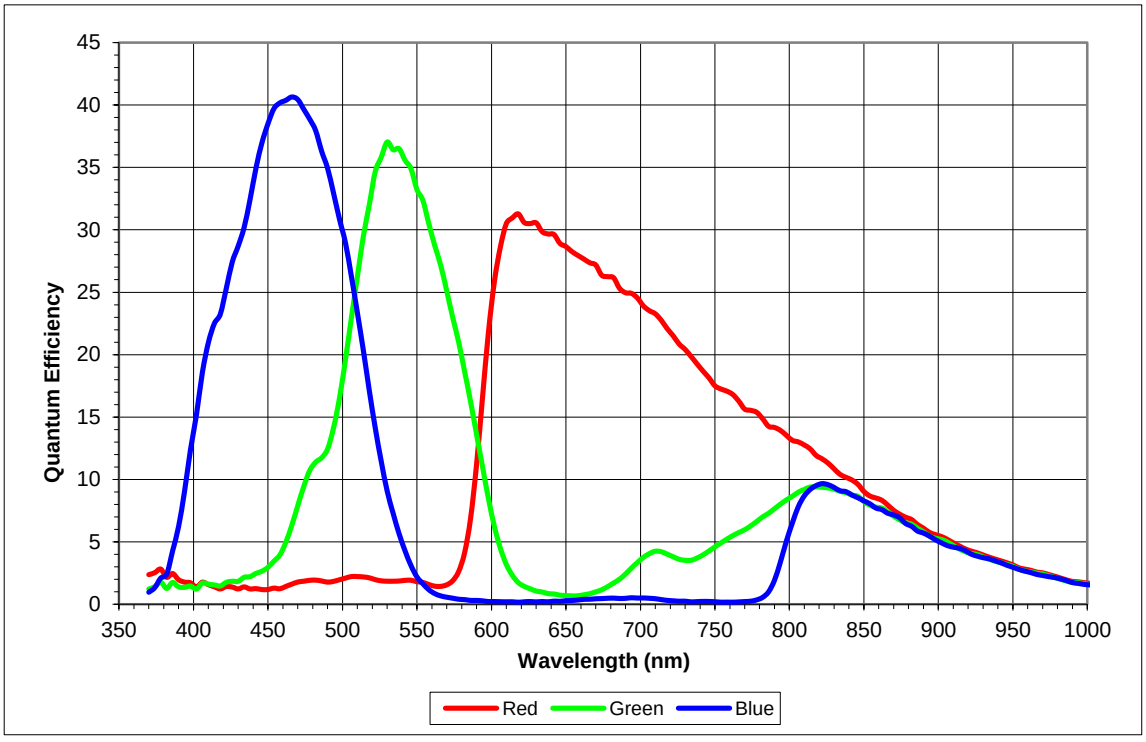


Figure 6: Color (Bayer RGB) Quantum Efficiency

PHOTORESPONSE VERSUS ANGLE

The horizontal curve is where the incident light angle is varied in a plane parallel to the HCCD.

The vertical curve is where the incident light angle is varied in a plane perpendicular to the HCCD.

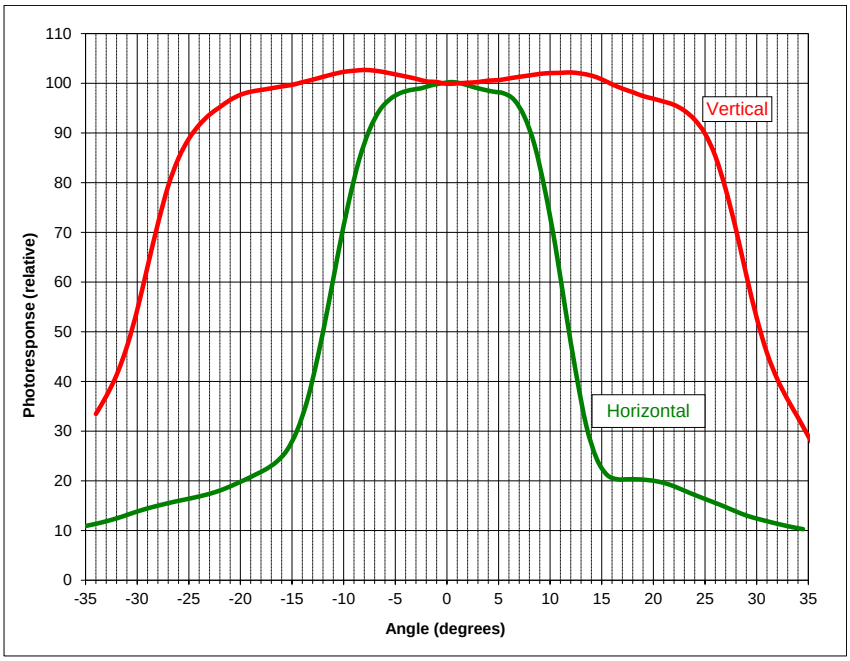


Figure 7: Photoresponse versus Angle

SENSOR POWER

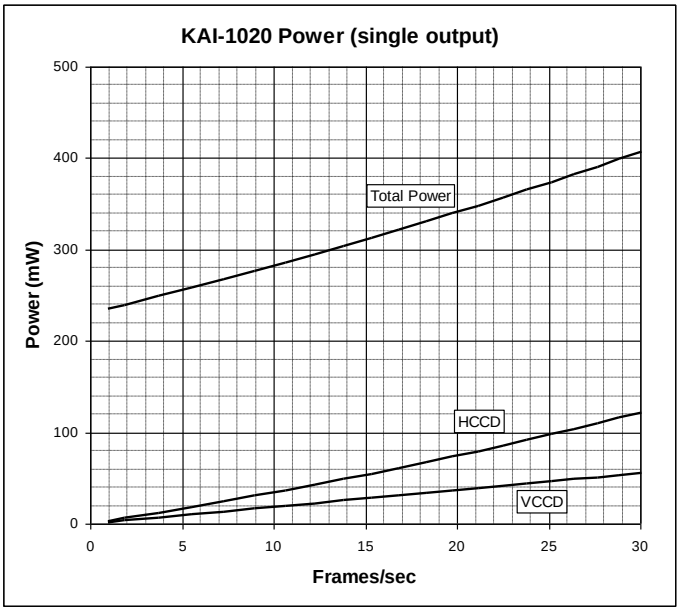


Figure 8: Power

FRAME RATE

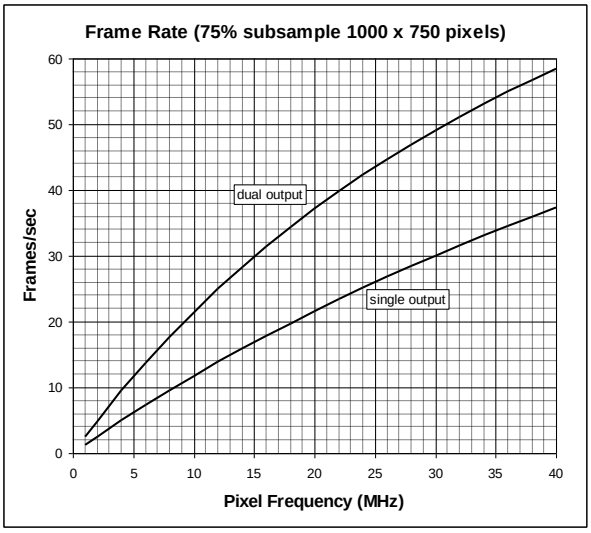


Figure 9: Frame Rate 1000 x 750 Pixels

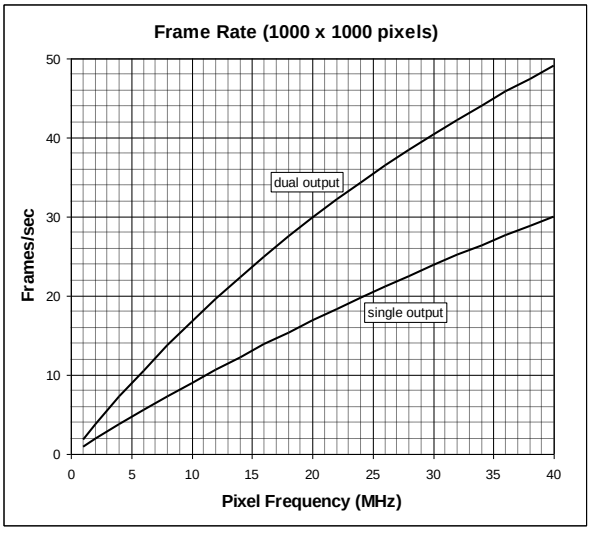


Figure 11: Frame Rate 1000 x 1000 Pixels

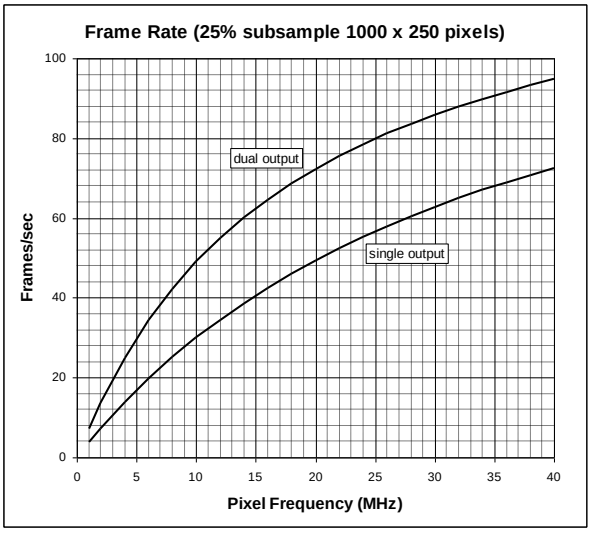


Figure 10: Frame Rate 1000 x 250 pixels

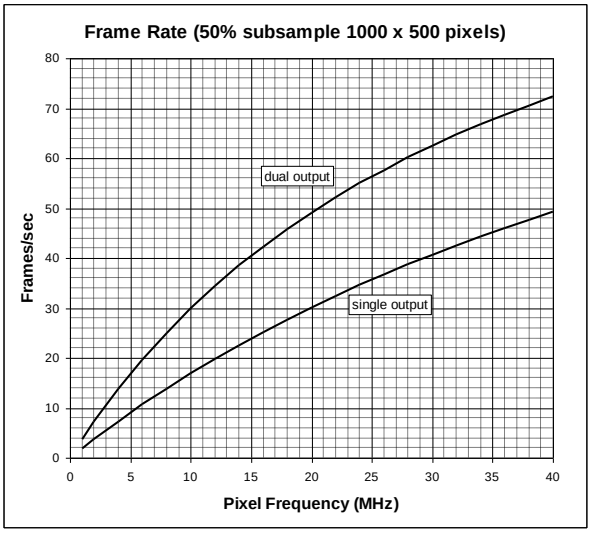


Figure 12: Frame Rate 1000 x 500 Pixels

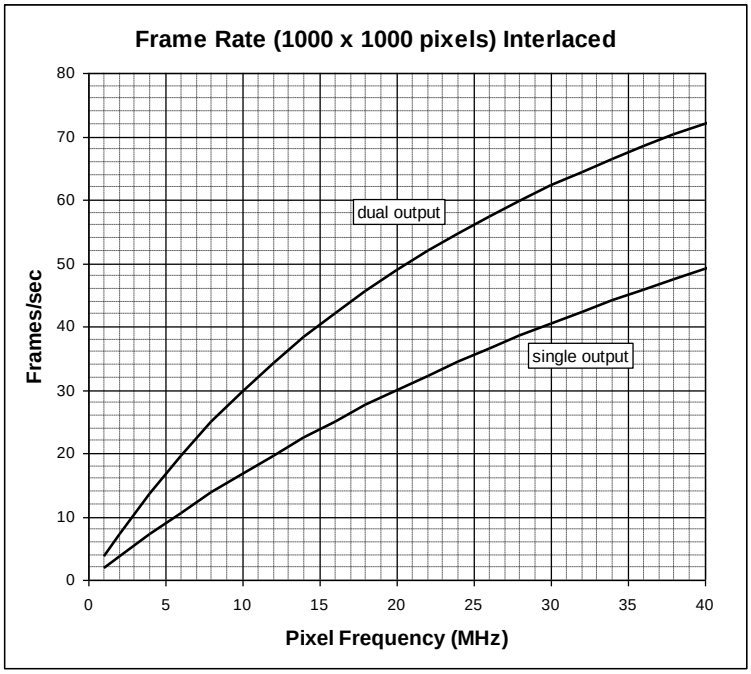


Figure 13: Frame Rate 1000 x 1000 Pixels Interlaced

Defect Definitions

SPECIFICATIONS

Name	Definition	Maximum	Temperature(s) tested at (°C)	Notes	Sampling Plan
Dark field major bright defective pixel	Defect ≥ 28mV	10	27, 40	1	Die
Bright field major dark or bright defective pixel	Defect ≥ 11%				Die
Bright field minor dark defective pixel	Defect ≥ 5%	20 in Zone 2	27, 40	8	Die
Dark field minor bright defective pixel	Defect ≥ 14mV	100	27, 40	2	Die
Bright field dead dark pixel	Defect ≥ 40%	0	27, 40	5	Die
Bright field nearly dead dark pixel	Defect ≥ 20%	0 in Zone 1 1 in Zone 2	27, 40	5, 8	Die
Dark field saturated bright pixel	Defect ≥ 106mV	0	27, 40	3	Die
Dark field minor cluster defect	A group of 2 to 10 contiguous dark field minor defective pixels	0	27, 40	4	Die
Bright field minor cluster defect	A group of 2 to 10 contiguous bright field minor defective pixels	2 in Zone 2	27, 40	4, 8	Die
Major cluster defect	A group of 2 to 10 contiguous major defective pixels	0	27, 40	4	Die
Column defect	A group of more than 10 contiguous major defective pixels along a single column	0	27, 40		Die
Column Average Magnitude	Within ± 0.4% of regional average (5 columns)	0	27, 40	6, 7	Die

Notes:

1. The defect threshold was determined by using a threshold of 8mV at an integration time of 33 milliseconds and scaling it by the actual integration time used of 117 msec. [8mV * (117 msec/ 33 msec) = 28 mV]
2. The defect threshold was determined by using a threshold of 4mV at an integration time of 33 milliseconds and scaling it by the actual integration time used of 117 msec. [4mV * (117 msec/ 33 msec) = 14 mV]
3. The defect threshold was determined by using a threshold of 30mV at an integration time of 33 milliseconds and scaling it by the actual integration time used of 117 msec. [30mV * (117 msec/ 33 msec) = 106 mV]
4. The maximum width of any cluster defect is 2 pixels.
5. Only dark defects.
6. Local average is centered on column.
7. See Test Regions of Interest for region used.
8. See Figure 17 for zone 1 and 2 definitions.

Defect Map

The defect map supplied with each sensor is based upon testing at an ambient (27°C) temperature. Minor point defects are not included in the defect map. All defective pixels are referenced to pixel 1, 1 in the defect map (see Figure 15: Regions of Interest).

Test Definitions

TEST CONDITIONS

Description	Condition	Notes
Frame time	117 msec	1
Horizontal clock frequency	10 MHz	
Light source (LED)	Continuous green illumination centered at 530 nm	2
Operation	Nominal operating voltages and timing	

Notes:
1. Electronic shutter is not used. Integration time equals frame time.
2. Green LED used: Nichia NSPG500S.

Test System Conversion Factors

KAI-1020 output sensitivity: 13 µV per electron

Test system gain (measured): 0.25 mV per ADU

Test system gain (calculated): 19 electrons per ADU

TESTS

Dark Field Center Uniformity

This test is performed under dark field conditions. Only the center 100 by 100 pixels of the sensor are used for this test (pixels 431, 431 to pixel 530, 530). See Figure 16.

$$\text{Dark field center uniformity} = \text{Standard Deviation of center 100 by 100 pixels in electrons} \times \left(\frac{\text{DPS Integration Time}}{\text{Actual Integration time used}}\right)$$

Units: e- rms. DPS integration time: Device Performance Specification Integration Time = 33 msec.

Dark Field Global Uniformity

This test is performed under dark field conditions. The sensor is partitioned into 100 sub regions of interest, each of which is 100 by 100 pixels in size. See Figure 14. The average signal level of each of the 100 sub regions of interest is calculated. The signal level of each of the sub regions of interest is calculated using the following formula:

$$\text{Signal of ROI}[i] = (\text{ROI Average in ADU} - \text{Horizontal overclock average in ADU}) * \text{mV per count}$$

Where i = 1 to 100. During this calculation on the 100 sub regions of interest, the maximum and minimum signal levels are found. The dark field global uniformity is then calculated as the maximum signal found minus the minimum signal level found.

Units: mVpp (millivolts peak to peak)

Global Uniformity

This test is performed with the light source illuminated to a level such that the output of the sensor is at 70% of saturation (approximately 364 mV). Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 520mV. Global uniformity is defined as:

$$\text{Global Uniformity} = 100 * \left(\frac{\text{Active Area Standard Deviation}}{\text{Active Area Signal}} \right)$$

Units: %rms. Active Area Signal = Active Area Average – Horizontal Overclock Average.

Global Peak to Peak Uniformity

This test is performed with the light source illuminated to a level such that the output of the sensor is at 70% of saturation (approximately 364 mV). Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 520mV. The sensor is partitioned into 100 sub regions of interest, each of which is 100 by 100 pixels in size. See Figure 14. The average signal level of each of the 100 sub regions of interest (ROI) is calculated. The signal level of each of the sub regions of interest is calculated using the following formula

Signal of ROI[i] = (ROI Average in ADU – Horizontal overclock average in ADU) * mV per count

Where i = 1 to 100. During this calculation on the 100 sub regions of interest, the maximum and minimum signal levels are found. The global peak to peak uniformity is then calculated as:

$$\text{Global Uniformity} = \frac{\text{Maximum Signal - Minimum Signal}}{\text{Active Area Signal}}$$

Units: %pp

Center Uniformity

This test is performed with the light source illuminated to a level such that the output of the sensor is at 70% of saturation (approximately 364 mV). Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 520mV. Defects are excluded for the calculation of this test. This test is performed on the center 100 by 100 pixels (See Test Regions of Interest and Figure 16) of the sensor. Center uniformity is defined as:

$$\text{Center ROI Uniformity} = 100 * \left(\frac{\text{Center ROI Standard Deviation}}{\text{Center ROI Signal}} \right)$$

Units: %rms. Center ROI Signal = Center ROI Average – Horizontal Overclock Average

Dark Field Defect Test

This test is performed under dark field conditions. The sensor is partitioned into 100 sub regions of interest, each of which is 100 by 100 pixels in size (see Figure 14). In each region of interest, the median value of all pixels is found. For each region of interest, a pixel is marked defective if it is greater than or equal to the median value of that region of interest plus the defect threshold specified.

Bright Field Defect Test

This test is performed with the light source illuminated to a level such that the output of the sensor is at 70% of saturation (approximately 364 mV). Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 520 mV. The average signal level of all active pixels is found. The bright and dark thresholds are set as:

Dark defect threshold = Active Area Signal * threshold

Bright defect threshold = Active Area Signal * threshold

The sensor is then partitioned into 100 sub regions of interest, each of which is 100 by 100 pixels in size. See Figure 14: Test Sub Regions of Interest. In each region of interest, the average value of all pixels is found. For each region of interest, a pixel is marked defective if it is greater than or equal to the median value of that region of interest plus the bright threshold specified or if it is less than or equal to the median value of that region of interest minus the dark threshold specified.

Example for major bright field defective pixels:

- Average value of all active pixels is found to be 365 mV.
- Dark defect threshold: 365mV * 11% = 40mV
- Bright defect threshold: 365mV * 11% = 40mV
- Region of interest #1 selected. This region of interest is pixels 1, 1 to pixels 100,100.
    - Median of this region of interest is found to be 366 mV.
    - Any pixel in this region of interest that is ≥ (366+40mV) 406mV in intensity will be marked defective.
    - Any pixel in this region of interest that is ≤ (366-40mV) 324mV in intensity will be marked defective.
- All remaining 99 sub regions of interest are analyzed for defective pixels in the same manner.

Bright Field Minor Defect Test

This test is performed with the light source illuminated to a level such that the output of the sensor is at 70% of saturation (approximately 364 mV). Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 520 mV. The average signal level of all active pixels is found. The dark threshold is set as:

Dark defect threshold = Active Area Signal * threshold

The sensor is then partitioned into 2500 sub regions of interest, each of which is 20 by 20 pixels in size. In each region of interest, the average value of all pixels is found. For each region of interest, a pixel is marked defective if it is less than or equal to the median value of that region of interest minus the dark threshold specified.

Example for bright field minor defective pixels:

- Average value of all active pixels is found to be 365 mV.
- Dark defect threshold: 365mV * 5% = 18mV
- Region of interest #1 selected. This region of interest is pixels 1, 1 to pixels 20, 20.
    - Median of this region of interest is found to be 366 mV.
    - Any pixel in this region of interest that is <= (366-18mV) 348mV in intensity will be marked defective.
- All remaining 2499 sub regions of interest are analyzed for defective pixels in the same manner.

Bright Field Column Average Magnitude Test

This test is performed with the light source illuminated to a level such that the output of the sensor is at 70% of saturation (approximately 364 mV). Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 520 mV. A column is marked as defective if

$$100 * \text{abs}\left(\frac{\text{Avg(Column n)} - \text{Avg(Avg(Column x))}}{\text{Avg(Avg(Column x))}}\right) > 0.4$$

Where x=n-2 to n+2

TEST REGIONS OF INTEREST

Number of pixels	1027 (H) x 1008 (V)
Number of photo sensitive pixels	1004 (H) x 1004 (V)
Number of active pixels	1000 (H) x 1000 (V)
Active Area ROI	Pixel (1, 1) to Pixel (1000, 1000)
Column Magnitude Test ROI	Pixel (11, 11) to Pixel (990, 990)

Notes:
1. Only the active pixels are used for performance and defect tests. See Figure 15.

Test Sub Regions of Interest

Pixel (1000,1000)

91	92	93	94	95	96	97	98	99	100
81	82	83	84	85	86	87	88	89	90
71	72	73	74	75	76	77	78	79	80
61	62	63	64	65	66	67	68	69	70
51	52	53	54	55	56	57	58	59	60
41	42	43	44	45	46	47	48	49	50
31	32	33	34	35	36	37	38	39	40
21	22	23	24	25	26	27	28	29	30
11	12	13	14	15	16	17	18	19	20
1	2	3	4	5	6	7	8	9	10

Pixel (1,1)

Figure 14: Test Sub Regions of Interest

Signal Level Calculation

Signal levels are calculated by using the average of the region of interest under test and subtracting off the horizontal overclock region. The test system timing is configured such that the sensor is overclocked in both the vertical and horizontal directions. See Figure 15 for a pictorial representation of the regions.

Example: To determine the active area average in millivolts, the following calculation used:

Active area signal (mV) = (Active area average – horizontal overclock average) * mV per count

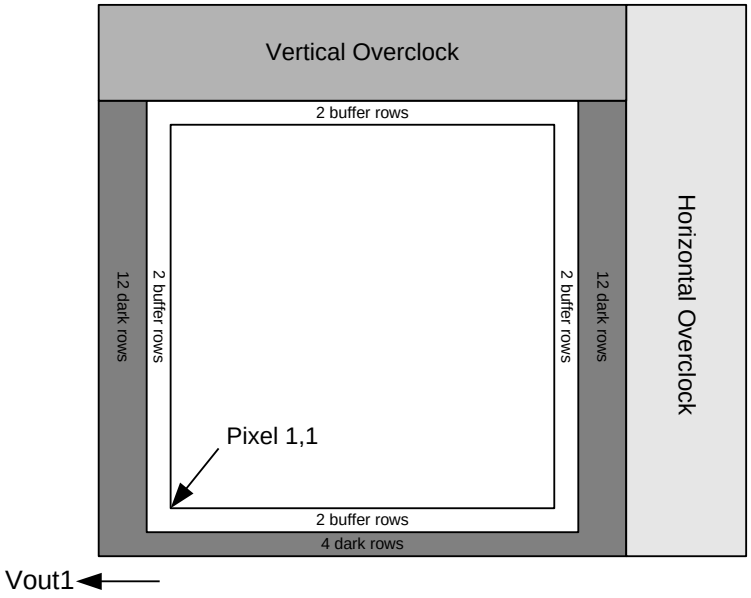


Figure 15: Regions of Interest

Center Region of Interest

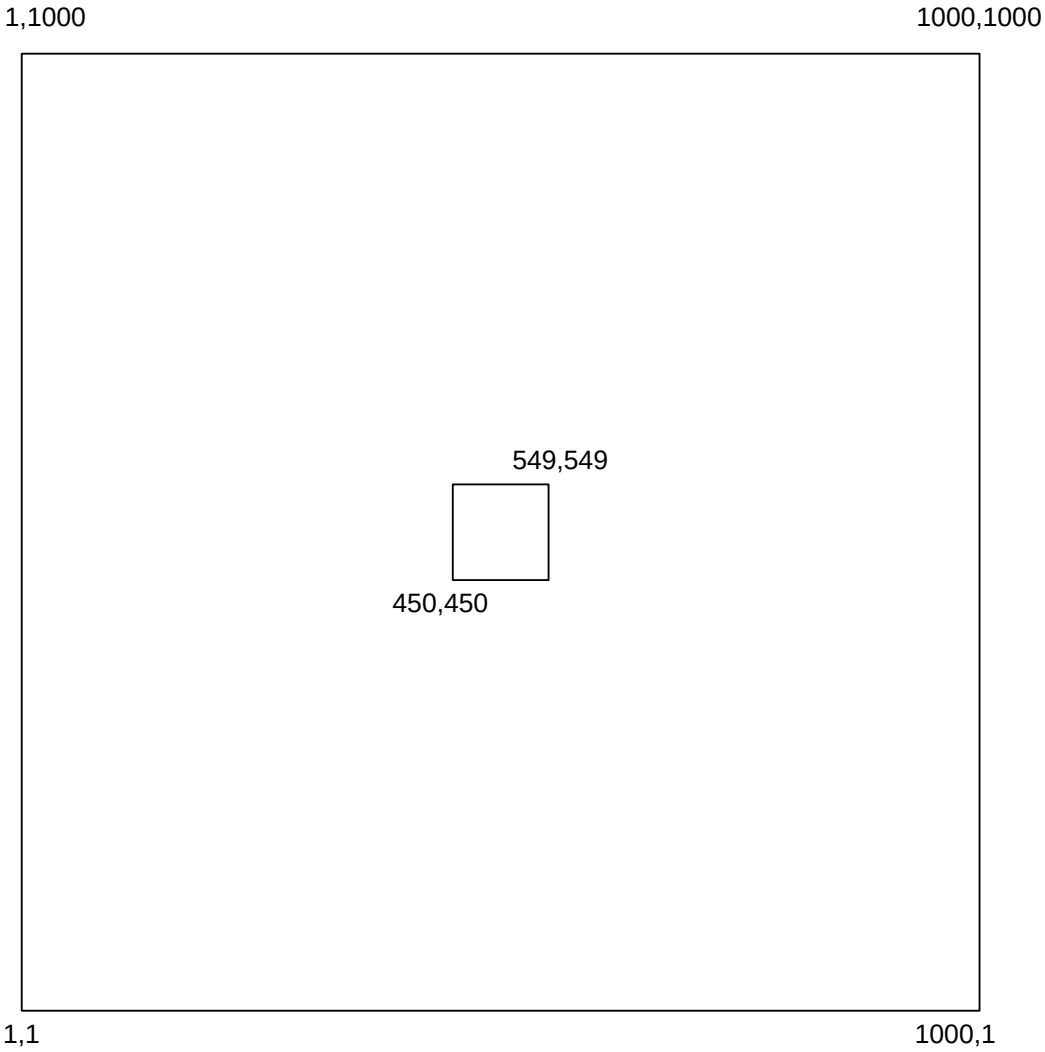


Figure 16: Center Region of Interest

Zones 1 and 2

Zone 2 includes zone 1

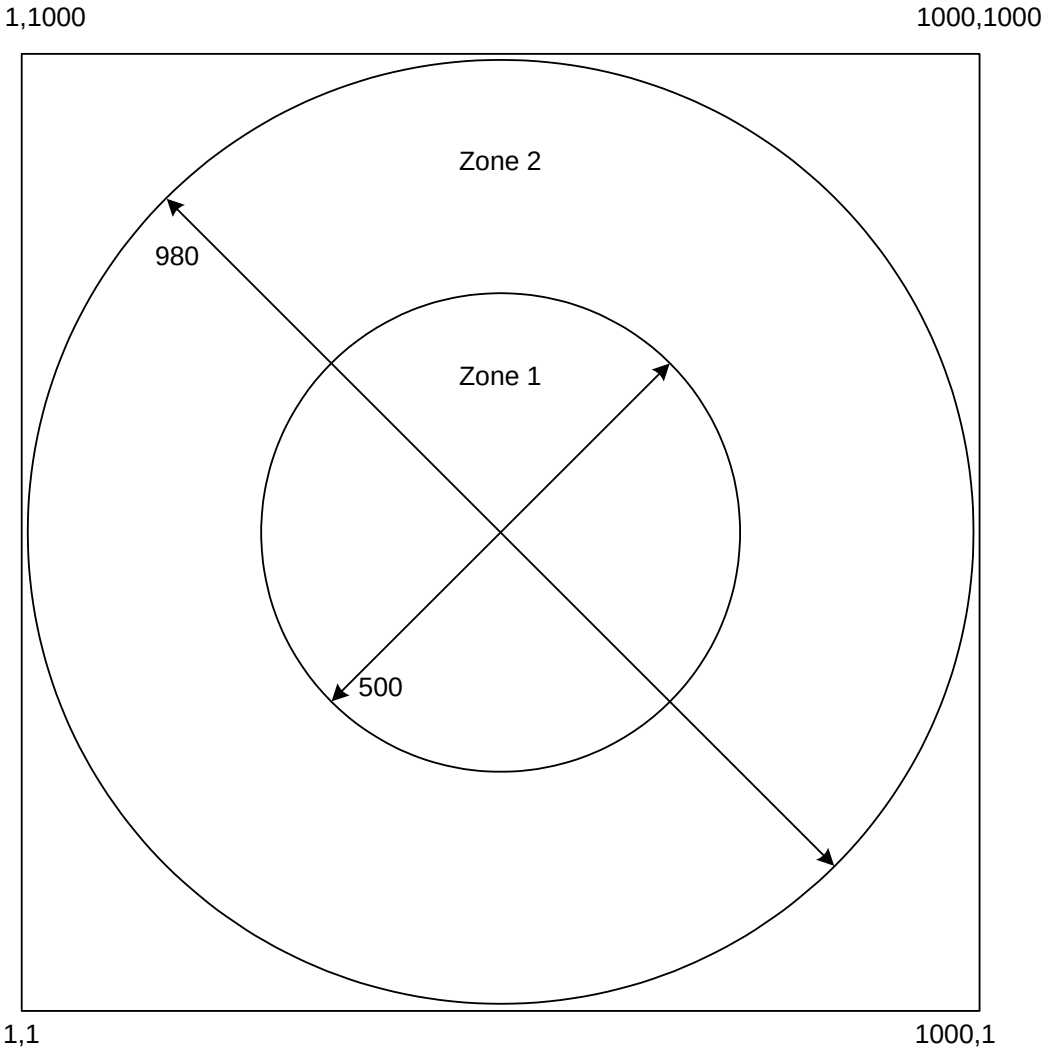


Figure 17: Zones 1 and 2

Operation

SINGLE OR DUAL OUTPUT

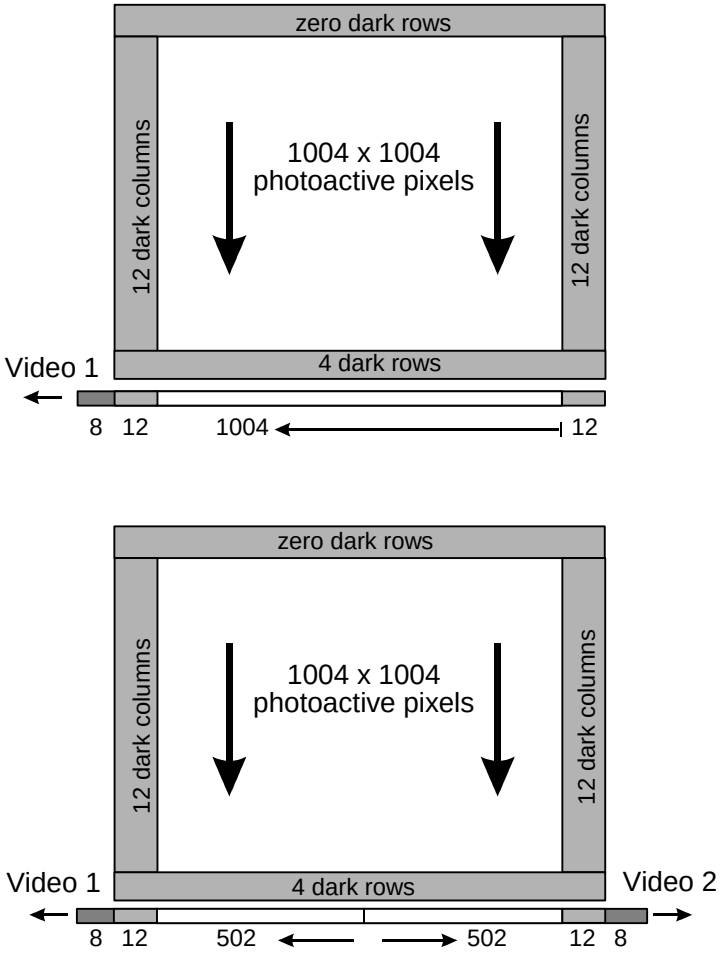


Figure 18: Single or Dual Output Mode of Operation

The KAI-1020 is designed to read the image out of one output at 30 frames/second or two outputs at 48 frames/second. In the dual output mode the right half of the horizontal shift register reverses its direction of charge transfer. The left half of the image is read out of video 1 and the right half of the image is read out of video 2.

There are no dark reference rows at the top and 4 dark rows at the bottom of the image sensor. The 4 dark rows should not be used for a dark reference level. The dark rows will contain smear signal from bright light sources. Use the 12 dark columns on the left or right side of the image sensor as a dark reference.

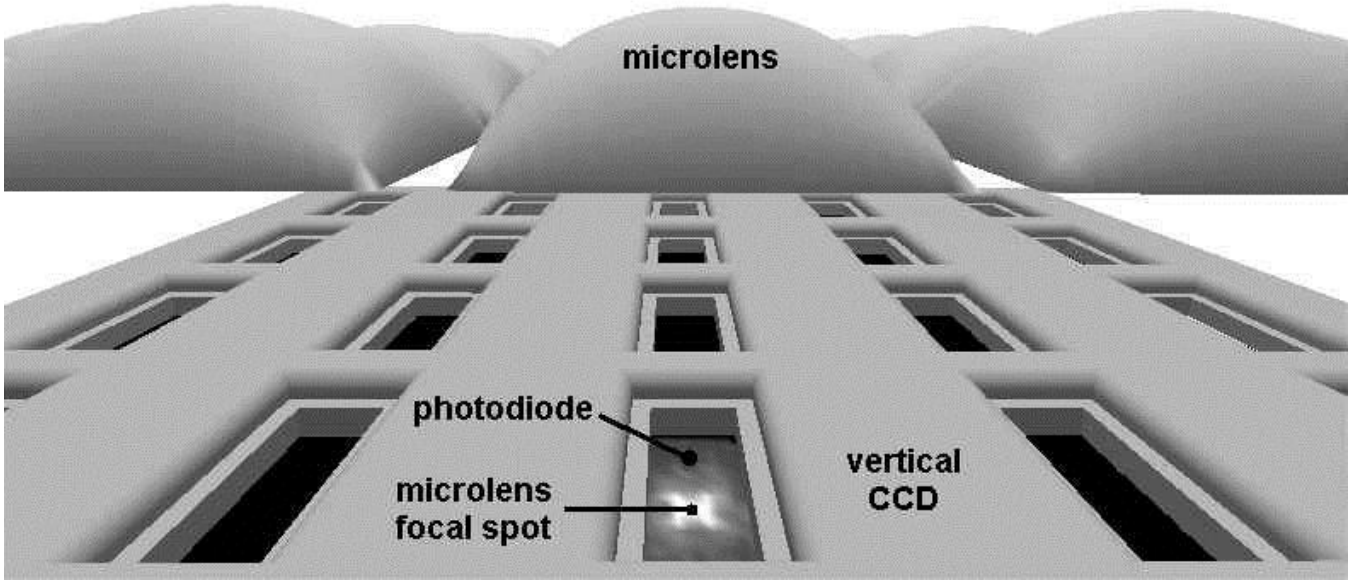


Figure 19: Pixel

THE KAI-1020 PIXEL

The pixel is 7.4 µm square. It consists of a light sensitive photodiode and an optically shielded vertical shift register. The vertical shift register is a charge-coupled device (VCCD). Each pixel is covered by a microlens to increase the light gathering efficiency of the photodiode.

Under normal operation, the image capture process begins with a 4 µs long pulse on the electronic shutter trigger input φSH. The electronic shutter empties all charge from every photodiode in the pixel array.

The photodiodes start collecting light on the falling edge of the φSH pulse. For each photon that is incident upon the 7.4 µm square area of the pixel, the probability of an electron being generated in the photodiode is given by the quantum efficiency (QE). At the end of the desired integration time, a 10 µs pulse on φV2B transfers the charge (electrons) collected in the photodiode into the VCCD. The integration time ends on the falling edge of φV2B.

HIGH LEVEL BLOCK DIAGRAM

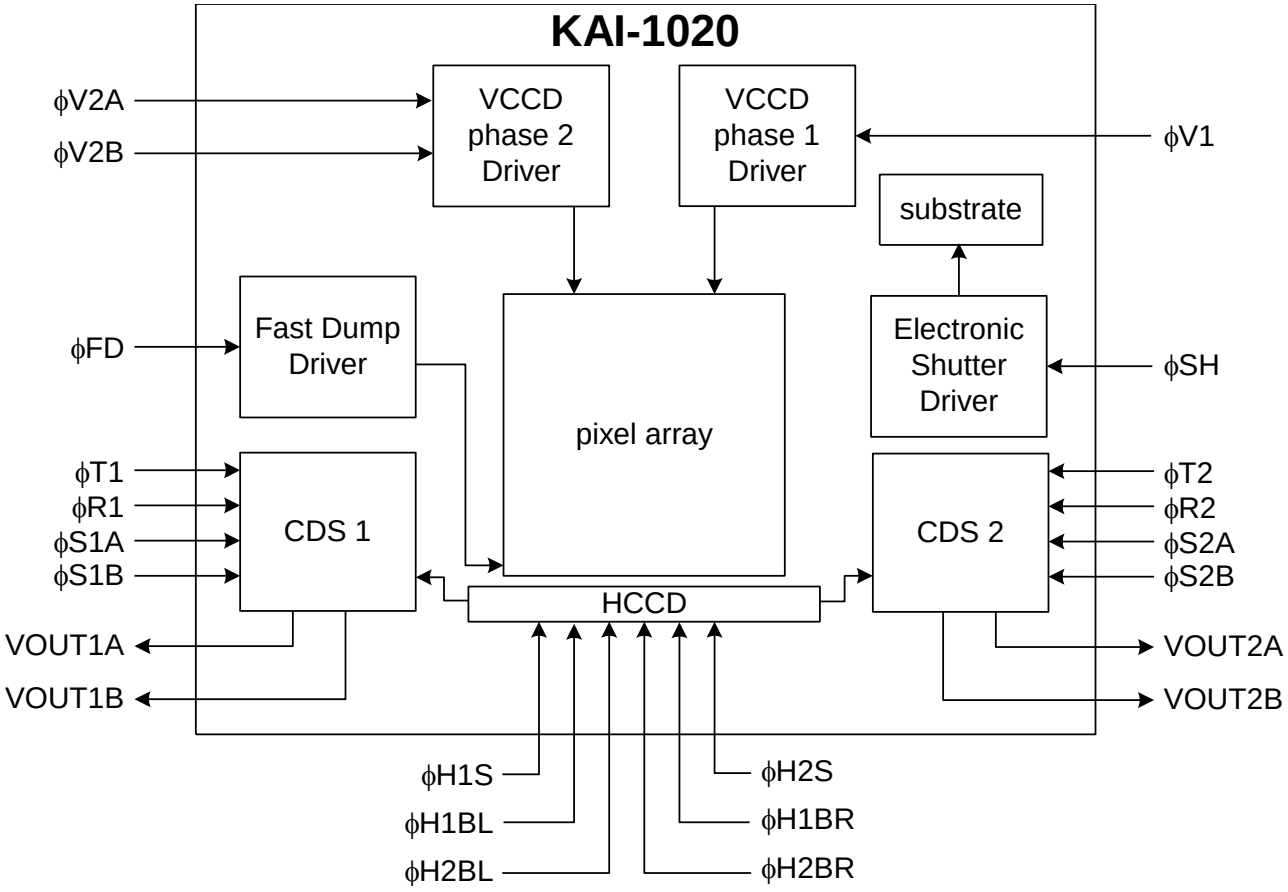


Figure 20: High Level Block Diagram

All timing inputs are driven by 5 V logic. The image sensor has integrated clock drivers to generate the proper voltages for the internal CCD gates. There are two VCCD clock drivers. Both the phase 1 and phase 2 VCCD drivers control the shifting of charge through the VCCD. The phase 2 driver also controls the transfer of charge from the photodiodes to the VCCD.

There is an integrated fast dump driver, which allows an entire row of pixels to be quickly discarded without clocking the row through the HCCD.

An integrated electronic shutter driver generates a >30 volt pulse on the substrate to simultaneously empty every photodiode on the image sensor.

Each of the two outputs has a correlated double sampling circuit to simplify the analog signal processing in the camera. The horizontal clock timing selects which outputs are active.

Main Timing

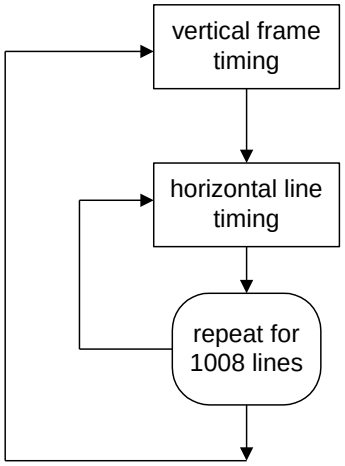


Figure 21: Timing Flow Chart

Vertical Frame Timing

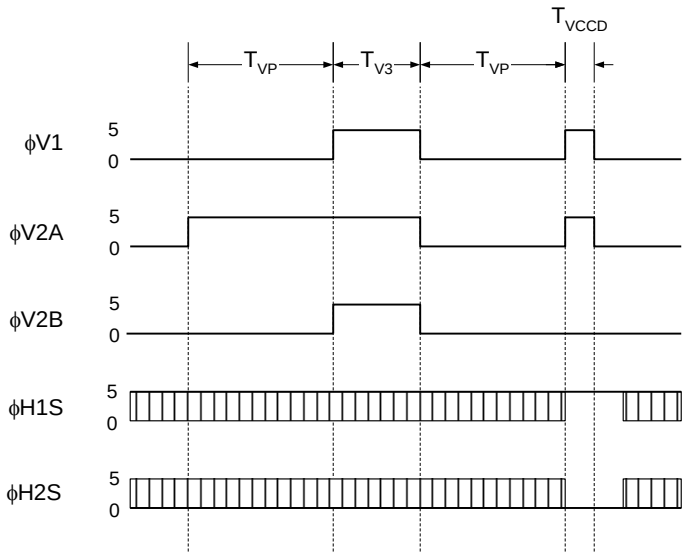


Figure 22: Vertical Frame Timing

The vertical frame timing may begin once the last pixel of the image sensor has been read out of the HCCD. The beginning of the vertical frame timing is at the rising edge of φV2A. After the rising edge of φV2A there must be a delay of TVP µs before a pulse of TV3 µs on φV2B and φV1. The charge is transferred from the photodiodes to the VCCD during the time TV3. The falling edge of φV2B marks the end of the photodiode integration time. After the pulse on φV2B the φV1 and φV2A should remain idle for T_{VP} µs before the horizontal line timing period begins. This allows the clock and well voltages time to settle for efficient charge transfer in the VCCD.

All HCCD and CDS timing inputs should run continuously through the vertical frame timing period. For an extremely short integration time, it is allowed to place an electronic shutter pulse on φSH at any time during the vertical frame timing. The φSH and φV2B pulses may be overlapped. The integration time will be from the falling edge of φSH to the falling edge of φV2B.

HORIZONTAL LINE TIMING

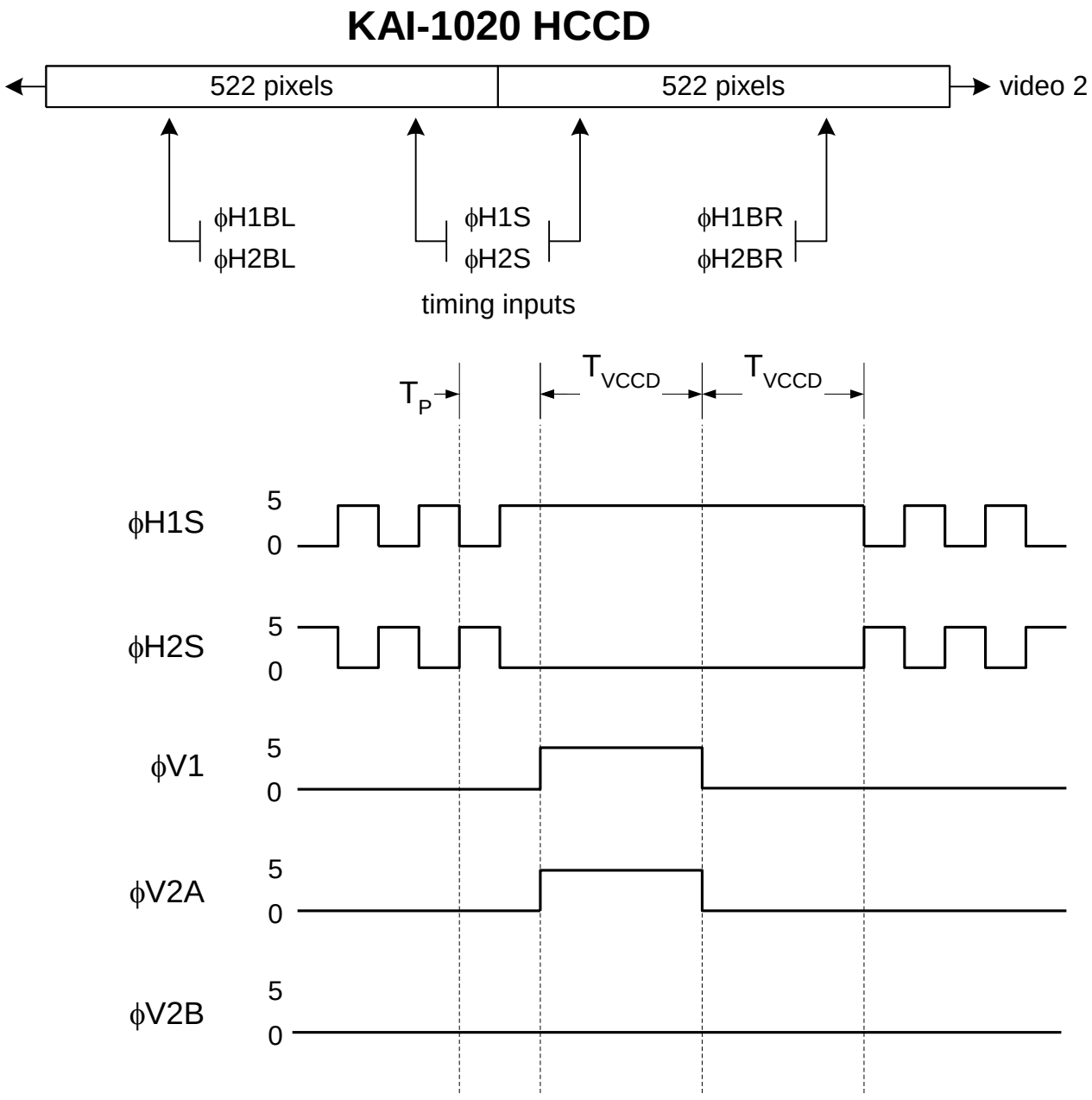


Figure 23: Horizontal Line Timing

When the φV2A and φV1 timing inputs are pulsed, charge in every pixel of the VCCD is shifted one row towards the HCCD. The last row next to the HCCD is shifted into the HCCD. When the VCCD is shifted, the timing signals to the HCCD must be stopped. φH1S must be stopped in the high state and φH2S must be stopped in the low state. The HCCD clocking may begin T_{VCCD} µs after the falling edge of the φV2A and φV1 pulse. The timing inputs to the CDS should run continuously through the horizontal line timing.

The HCCD has a total of 1036 pixels. The 1028 vertical shift registers (columns) are shifted into the center 1028 pixels of the HCCD. There are 8 pixels at both ends of the HCCD which receive no charge from a vertical shift register. The first 8 clock cycles of the HCCD will be empty pixels (containing no electrons). The next 12 clock cycles will contain only electrons generated by dark current in the VCCD and photodiodes. The next 1004 clock cycles will contain photo-electrons (image data). Finally, the last 12 clock cycles will contain only electrons generated by dark current in the VCCD and photodiodes. Of the 12 dark columns, the first and last dark columns should not be used for determining the zero signal level. Some light does leak into the first and last dark columns. Only use the center 10 columns of the 12 column dark reference.

When the HCCD is shifting valid image data, the timing inputs to the electronic shutter driver (φSH), VCCD driver (φV2A, φV2B, φV1), and fast dump drivers (φFD) should be held at the low level. This prevents unwanted noise from being introduced into the CDS circuit.

The HCCD is a type of charge coupled device known as a pseudo-two phase CCD. This type of CCD has the ability to shift charge in two directions. This allows the entire image to be shifted out to the video 1 output CDS, or to the video 2 output CDS (left/right image reversal). The HCCD is split into two equal halves of 522 pixels each. When operating the sensor in single output mode the two halves of the HCCD are shifted in the same direction. When operating the sensor in dual output mode the two halves of the HCCD are shifted in opposite directions. The direction of charge transfer in each half is controlled by the φH1BL, φH2BL, φH1BR, and φH2BR timing inputs.

Single Output

To direct all pixels to the video 1 output make the following HCCD connections:

φH1S = φH1BL, φH2BR

φH2S = φfH2BL, φH1BR

To direct all pixels to the video 2 output make the following HCCD connections:

φH1S = φH2BL, φH1BR

φH2S =φfH1BL, φH2BR

In each case the first 8 pixels will contain no electrons, followed by 12 dark reference pixels containing only electrons generated by dark current, followed by 1004 photo-active pixels, followed by 12 dark reference pixels. The HCCD must be clocked for at least 1028 cycles. The VCCD may be clocked immediately after the 1028th HCCD clock cycle.

If the sensor is to be permanently operated in single output mode through video 1, then VDD2 (pins B8, and B10) may be connected to GND. This disables the video 2 CDS and lowers the power consumption.

If the sensor is to be permanently operated in single output mode through video 2, then VDD1 and VDD2 supplies must be +15 V. The VDD1 supplies must always be at +15 V for the sensor to operate properly.

Dual Output

To use both outputs for faster image readout, make the following HCCD connections:

φH1S = φH1BL, φH1BR

φH2S = φH2BL, φH2BR

For both outputs the first 8 HCCD clock cycles contain no electrons, followed by 12 dark reference pixels containing only dark current electrons, followed by 502 photo-active pixels. This adds up to 522 pixels, but the HCCD should be clocked for at least 523 cycles before the next VCCD line shift takes place. The extra HCCD clock cycle ensures that the signal from the last pixel exits the CDS circuit before the VCCD drivers switch the gate voltages. This extra cycle is not needed for the single output modes because in that case, the last pixel is from a column of the dark reference which is not used. See the section on correlated double sampling for a description of the one pixel delay in the CDS circuit.

ELECTRONIC SHUTTER

Substrate Voltage

The voltage on the substrate, pins L1 and L5, determines the charge capacity of the photodiodes. When VSUB is 8 volts the photodiodes will be at their maximum charge capacity. Increasing VSUB above 8 volts decreases the charge capacity of the photodiodes until 30 volts when the photodiodes have a charge capacity of zero electrons. Therefore, a short pulse on VSUB, with a peak amplitude greater than 30 volts, empties all photodiodes and provides the electronic shuttering action.

Substrate Voltage and Antiblooming

It may appear the optimal substrate voltage setting is 8 volts to obtain the maximum charge capacity and dynamic range. While setting VSUB to 8 volts will provide the maximum dynamic range, it will also provide the minimum antiblooming protection.

The KAI-1020 VCCD has a charge capacity of 60,000 electrons (60 ke^-). If the VSUB voltage is set such that the photodiode holds more than 60 ke^-, then when the charge is transferred from a full photodiode to VCCD, the VCCD will overflow. This overflow condition manifests itself in the image by making bright spots appear elongated in the vertical direction. The size increase of a bright spot is called blooming when the spot doubles in size.

The blooming can be eliminated by increasing the voltage on VSUB to lower the charge capacity of the photodiode. This ensures the VCCD charge capacity is greater than the photodiode capacity. There are cases where an extremely bright spot will still cause blooming in the VCCD. Normally, when the photodiode is full, any additional electrons generated by photons will spill out of the photodiode. The excess electrons are drained harmlessly out to the substrate. There is a maximum rate at which the electrons can be drained to the substrate.

If that maximum rate is exceeded, (say, for example, by a very bright light source) then it is possible for the total amount of charge in the photodiode to exceed the VCCD capacity. This results in blooming.

The amount of antiblooming protection also decreases when the integration time is decreased.

There is a compromise between photodiode dynamic range (controlled by VSUB) and the amount of antiblooming protection. A low VSUB voltage provides the maximum dynamic range and minimum (or no) antiblooming protection. A high VSUB voltage provides lower dynamic range and maximum antiblooming protection. The optimal setting of VSUB is written on the container in which each KAI-1020 is shipped. The given VSUB voltage for each sensor is selected to provide antiblooming protection for bright spots at least 100 times saturation, while maintaining at least 500 mV of dynamic range.

A detailed discussion of antiblooming and smear may be found in IEEE Transactions on Electron Devices vol. 39 no. 11, pg. 2508.

Extremely bright light can potentially harm solid state imagers such as Charge-Coupled Devices (CCDs). Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions*.

Electronic Shutter Timing

The electronic shutter provides a method of precisely controlling the image exposure time without any mechanical components. If an integration time of T_{INT} is desired, then the substrate voltage of the sensor is pulsed to at least 30 volts T_{INT} seconds before the photodiode to VCCD transfer pulse on φV2B. The large substrate voltage pulse is generated by the KAI-1020. The electronic shutter is triggered by a 5 volt pulse on φSH. Use of the electronic shutter does not have to wait until the previously acquired image has been completely read out of the VCCD. The electronic shutter pulse may be added to the end of the horizontal line timing and just after the last pixel has been read out of the HCCD. φH1S and φH2S must be clocked during the electronic shutter pulse.

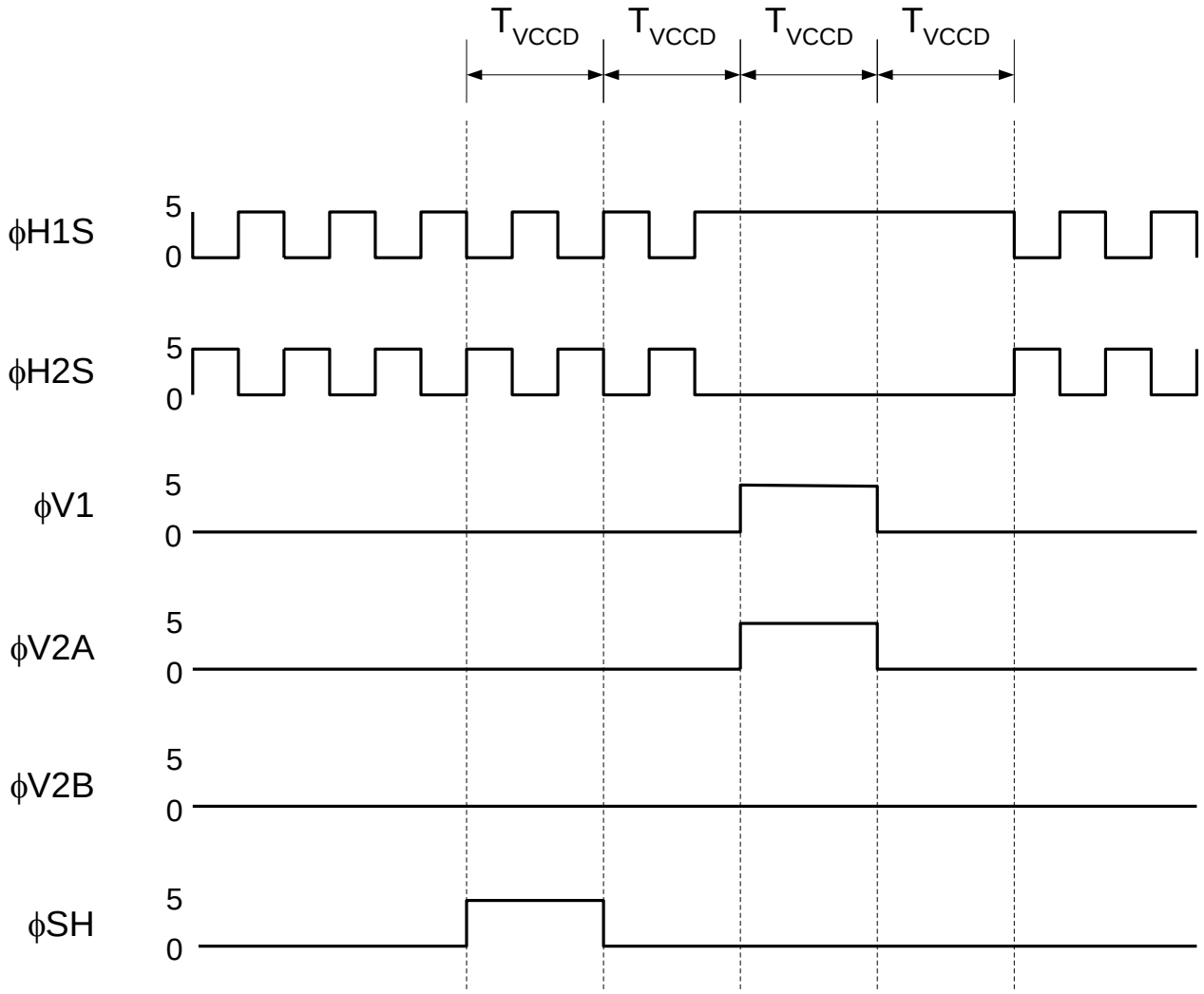


Figure 24: Electronic Shutter Timing

FAST DUMP

The KAI-1020 has the ability to rapidly discard (fast dump, FD) entire lines of the image. The fast dump is a drain attached to the last row of the VCCD just before the HCCD. When the fast dump is activated by taking φFD high, charge from the VCCD goes into the drain instead of into the HCCD.

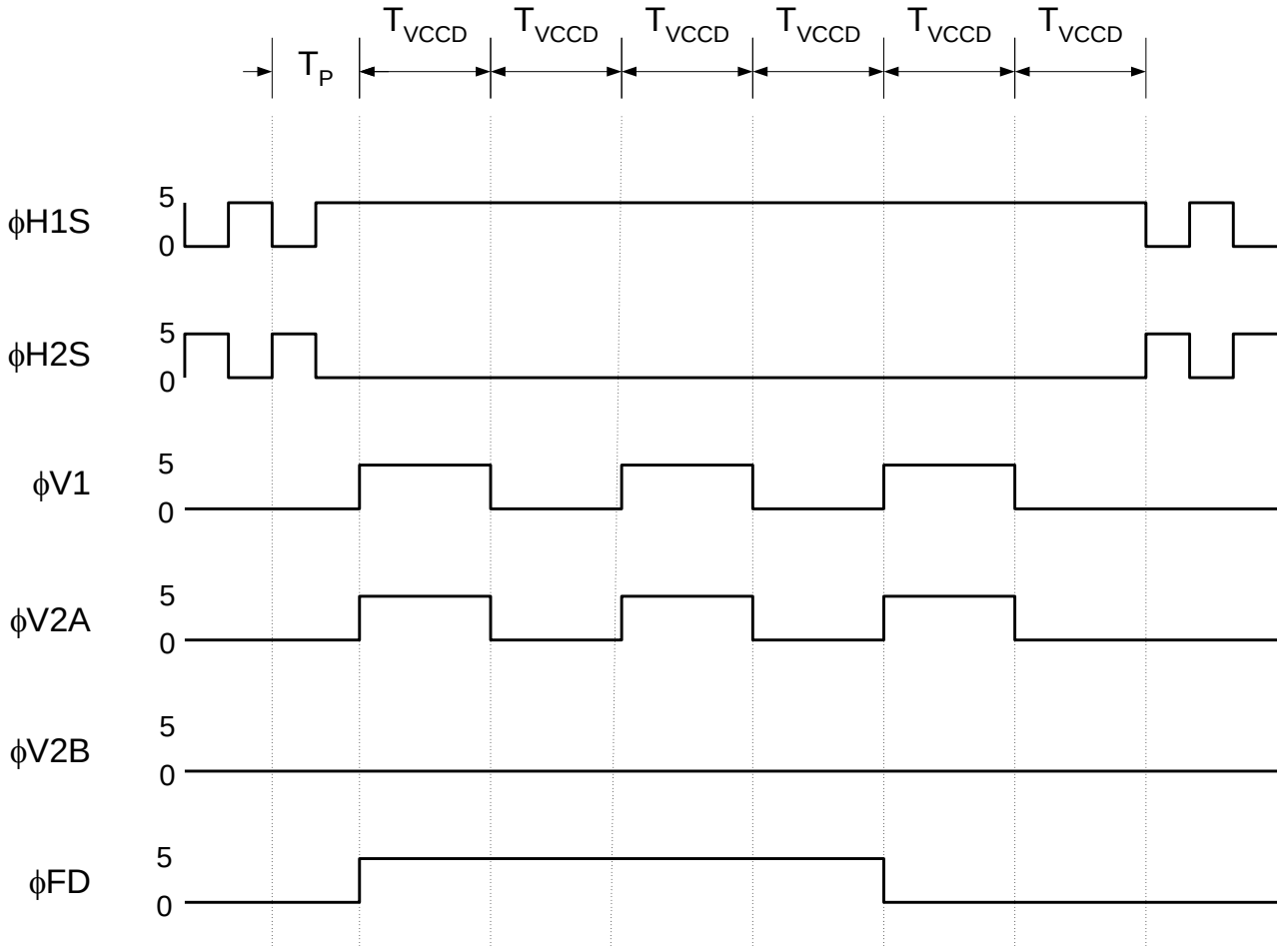


Figure 25: Fast Dump timing

This timing diagram shows how two lines are dumped and the third is read out. φFD should go high once the last pixel of the preceding line has been read out. Cycle the VCCD for the number of rows to be dumped. The above timing diagrams shows two rows being dumped. When the proper number of rows have been dumped bring φFD low. Then clock the VCCD through one more cycle to shift a row into the HCCD.

The fast dump can be used to sub-sample the image for increased frame rates. For example, by dumping the even numbered lines, the image will be sub-sampled by a factor of 2 and the frame rate will almost increase by a factor of 2. Horizontal sub-sampling is not possible. The HCCD must always be cycled for the entire number of pixels in one line.

Another way to increase the frame rate is through sub-windowing. For example, suppose only the center 512 lines of the image are needed. Turn on the fast dump and clock the VCCD for 256 lines. Then turn off the fast dump and clock the VCCD (and HCCD) for 512 lines. Finally, turn the fast dump on again and clock the VCCD for 240 lines.

BINNING AND INTERLACED MODES

Binning is a readout mode of progressive scan CCD image sensors where more than one row at a time is clocked into the HCCD before reading out the HCCD. This timing mode sums two or more rows together. It increases the frame rate because there are fewer total rows to read out of the HCCD. The following timing diagram shows how two rows are summed together:

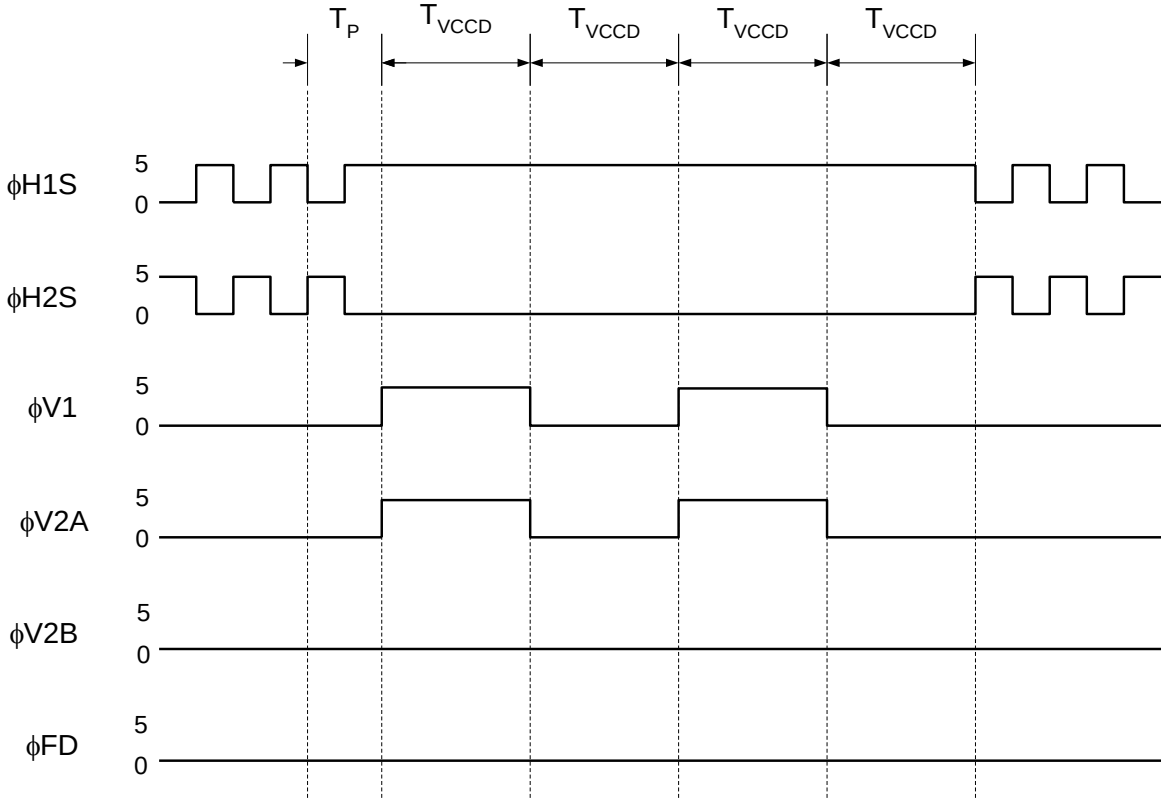


Figure 26: Binning Line Timing

When binning two rows together only 504 rows need to be read out of the HCCD instead of the normal 1008 rows. The HCCD will hold up to two VCCD rows of full signal without blooming. Binning more than two rows may cause horizontal blooming for saturated signal levels.

Interlaced readout is a form of binning. To read out the even field use binning to sum together rows 0+1, rows 2+3, ... rows 1006+1007. To read out the odd field use binning to read out rows 0+1+2, rows 3+4, rows 5+6, ... rows 1005+1006, rows 1007+1008. The odd field may also be read out as row 0, rows 1+2, rows 3+4, ... rows 1005+1006. See the Interlaced – Field Integration section for an example of interlaced timing.

CORRELATED DOUBLE SAMPLING (CDS)

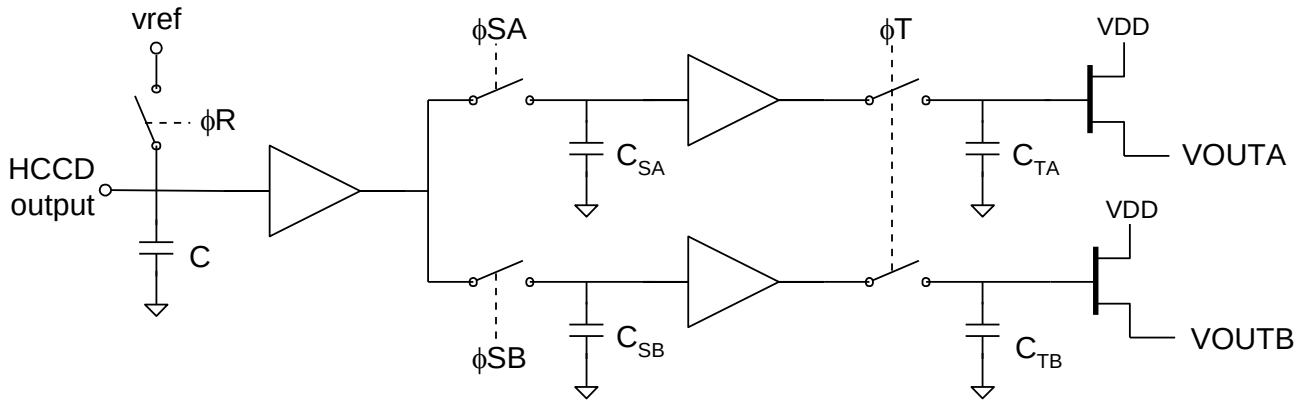


Figure 27: Correlated Double Sampling Block Diagram

Correlated double sampling is a method of measuring the amount of charge in each pixel. The electrons in the last pixel of the HCCD are transferred onto a very small sensing capacitor, C, on the falling edge of φH2S. The voltage on C will change by about 20 µV for each electron that was in the HCCD. The process of measuring the amount of charge begins by resetting the value of C to an internally generated reference voltage, vref. A short pulse on φR at the rising edge of φH2S will reset C. After C has been reset, its voltage is sampled and stored on C_{SA} by a short pulse on switch φSA. Then on the falling edge of φH2S, electrons are transferred onto the capacitor, C. The new voltage on C is sampled and stored on CSB by a short pulse on switch φSB. These two sampled voltages are then transferred to capacitors CTA and CTB by a short pulse on φT. φT and φR generally occur at the same time. An external operational amplifier is used to subtract the two voltages on VOUTA and VOUTB. The output of the op-amp will be proportional to the number of electrons contained in one pixel. Note that it takes one entire pixel clock cycle for the value of the pixel to appear on VOUTA and VOUTB. The A and B outputs of the CDS circuit will be in the range of 7 to 11 volts.

CDS Timing Edge Alignment

1. The edge alignments of the CDS timing pulses φSA, φSB, φT, and φR are critical to proper operation of the CDS circuit.
2. The falling edge of φR must not overlap the rising edge of φSA
3. The falling edge of φSA must come at the same time or before the falling edge of φH2
4. The rising edge of φSB must come after the falling edge of φH2
5. The falling edge of φSB must come before the rising edge of φR
6. The rising edge of φR may come before the rising edge of φH2
7. φT should always be driven by the same timing signal as φR
8. The pulse widths should be set such that φR, φSA, and φSB are 1/3 of T_P

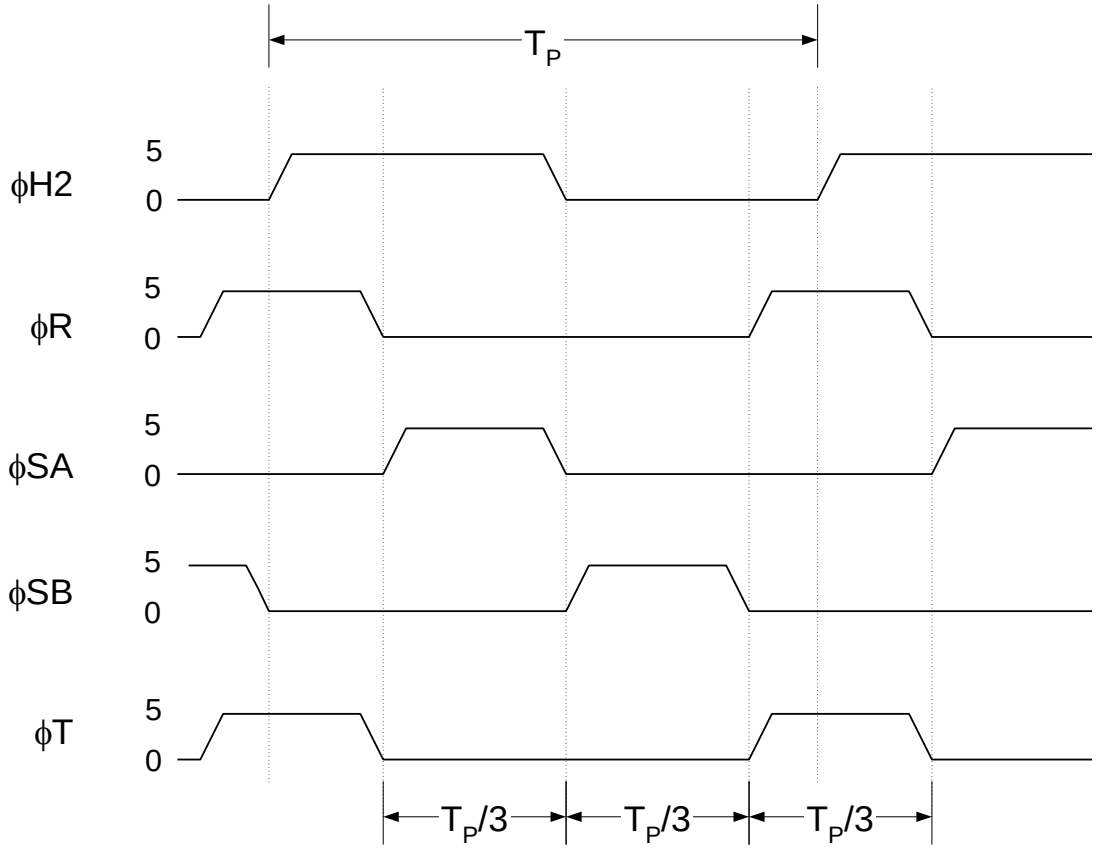


Figure 28: Correlated Double Sampling Timing

Disabling the CDS

There may be instances when the camera designer may want to use an external CDS. Such cases may occur at pixel clock frequencies 20MHz or slower where integrated CDS, analog to digital converter (A/D), and auto offset/gain circuits are available. These external CDS circuits require the raw unprocessed video waveform. The raw video can be obtained by permanently turning on the φSA, φSB, and φT switches by connecting them to a voltage in the range of 8 to 10V (the V2HIGH supply voltage, for example). Then place a load of 4 mA to 5 mA on VOUTA and a load of 0.1mA on VOUTB. VOUTA will be the raw video output suitable for external CDS circuits. The 5mA load may be a 2.0kΩ resistor and the 0.1 mA load may be an 80kΩ resistor to GND. An external CDS is not recommended for pixel frequencies above 20MHz.

TIMING AND VOLTAGE SPECIFICATIONS

Absolute Maximum Ratings

		Min.	Max.	Units	Notes
Temperature	Operation without damage	-50	70	C	
	Storage	-55	70	C	
Voltage between pins	VSUB to GND	8	20	V	1
	VDD to GND	0	17	V	
	φV1 to φV2, φFD to φV1, φV2	-10	10	V	
	φH1 to φH2	-8	8	V	
	φR, φT, φSA, φSB to GND	-9	12	V	
	φH1, φH2 to φV1, φV2	-9	10	V	
Current	Video Output Bias Current	0	7	mA	2

Notes:
1. For electronic shuttering VSUB may be pulsed to 35 V for up to 10 µs.
2. Note that the current bias affects the amplifier bandwidth.

Timing

Time	Min.	Nominal	Max.	Units
TP	25	25	500	ns
TVCCD	3.6	3.6	10	µs
TVP	20	25	40	µs
TV3	8	10	15	µs

Bias Voltages

Bias	Min (Volts)	Nominal (Volts)	Max (Volts)	Peak Current (mA)	Peak Current Frequency	Avg. Current (mA)
V1S5	4	5	6	2	2L	0.13
V1MID	-1.5	-1.2	-1.0	110	L	3
V1LOW	-9.5	-9	-8.5	110	L	3
V2S5	4	5	6	2	2L	0.5
V2S9	8	9	10	2	F	0.3
V2HIGH	8	9	10	110	L	0.01
V2MID	-1.5	-1.2	-1.0	110	L	3
V2LOW	-9.5	-9	-8.5	110 220	L F	3.8
VDD1	14.5	15	15.5			14
VDD2	14.5	15	15.5			14
VSH15	14	15	16	1	F	0.08
VSUB	8	*	14			0.03

Notes:
1. Average currents are for 30 frames/second
2. Peak switching currents are for less than 1 µs duration
3. L = once per line time, 2L = twice per line time, F = once per frame time
4. Substrate bias voltage for a 500mV output range is written on the shipping container for each part

Power Up Sequence

1. Power up VSUB, V1LOW, V2LOW first
2. Then power up VDD, VSH15, V2S5, V1S5, V1MID, V2MID and V2HIGH
3. Then after the coupling capacitors on all of the timing inputs have charged, begin clocking the timing inputs.

Any positive voltage should never be allowed to go negative. Any negative voltage should never be allowed to go positive.

Note that the shutter driver clock input does not use a coupling capacitor. It must be driven directly from a 5V logic buffer as shown in the evaluation board schematic.

Pulse Amplitudes

Clock	Min. Amplitude (volts)	Coupling	Min. Coupling Capacitor Value (µF)	Max. Coupling Capacitor Value (µF)
φSH	3.5	DC	--	--
φH1	4.7	AC	0.1	0.47
φH2	4.7	AC	0.1	0.47
φSA	4.7	AC	0.01	0.47
φSB	4.7	AC	0.01	0.47
φR	4.7	AC	0.01	0.47
φT	4.7	AC	0.01	0.47
φV1	4.0	AC	0.01	0.47
φV2A	4.0	AC	0.01	0.47
φV2B	4.0	AC	0.01	0.47
φFD	4.0	AC	0.1	0.47

TIMING EXAMPLES

Progressive Scan

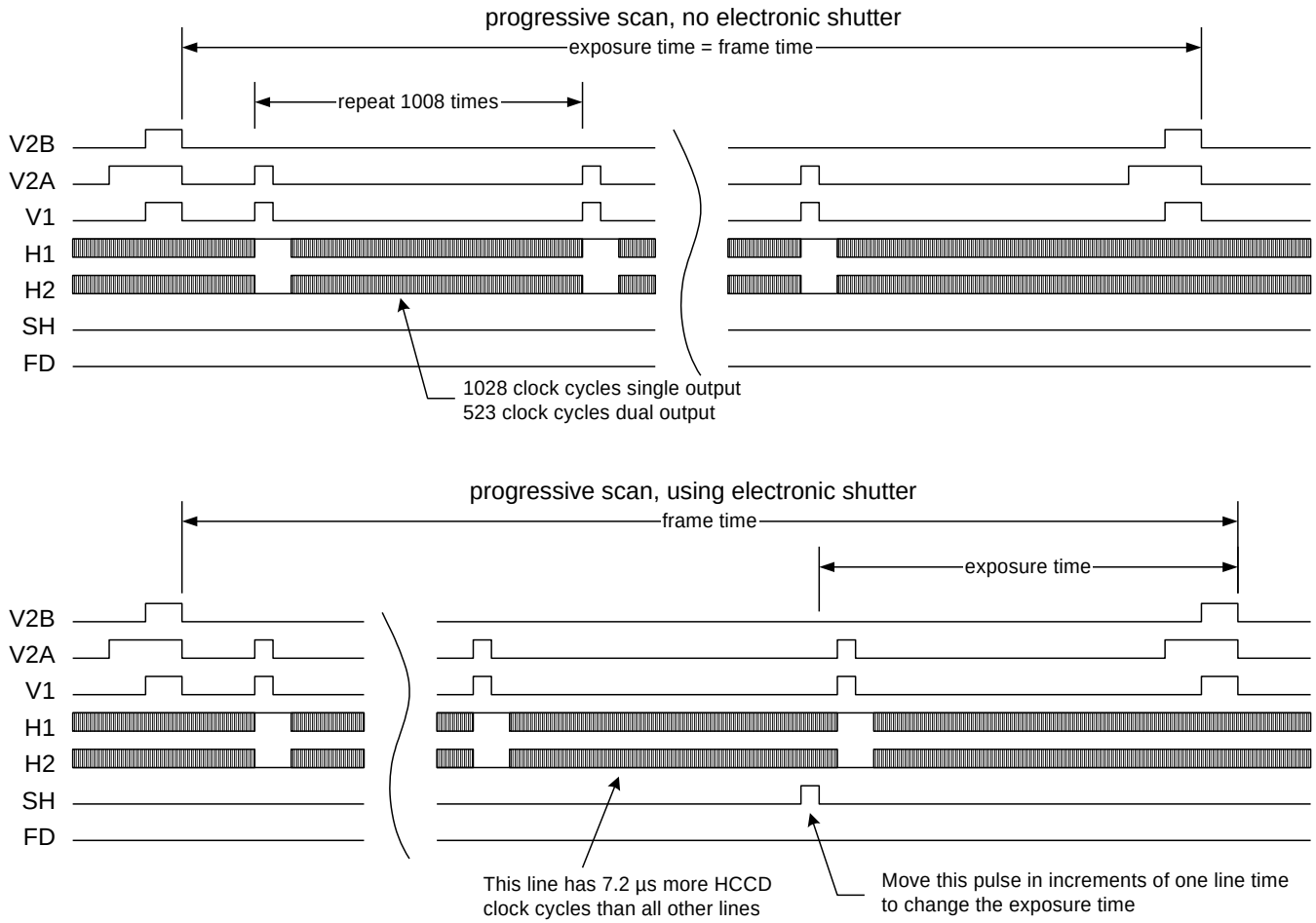


Figure 29: Progressive Scan Timing Example

Fast Line Dump

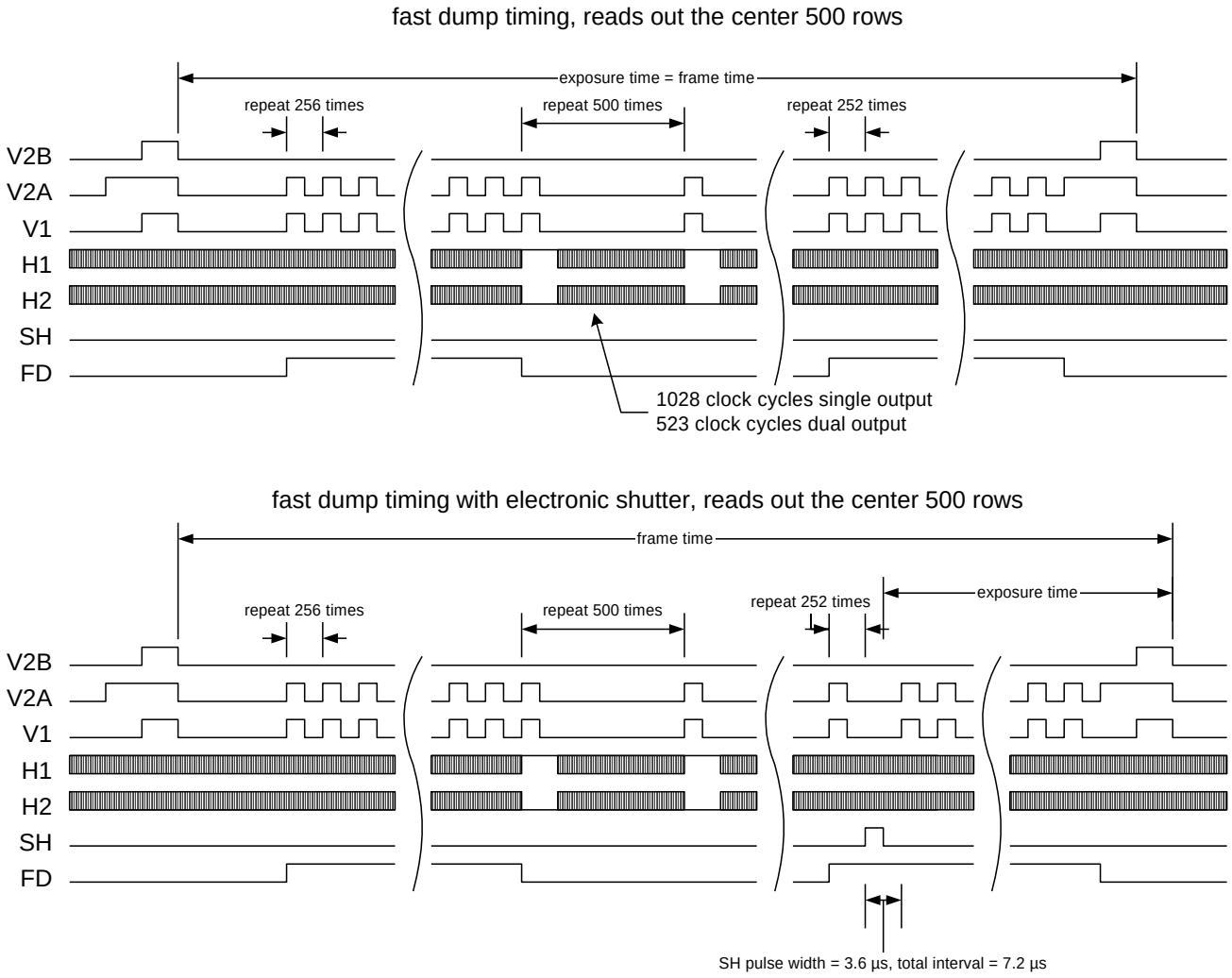


Figure 30: Fast Line Dump Timing Example

Interlaced – Field Integration

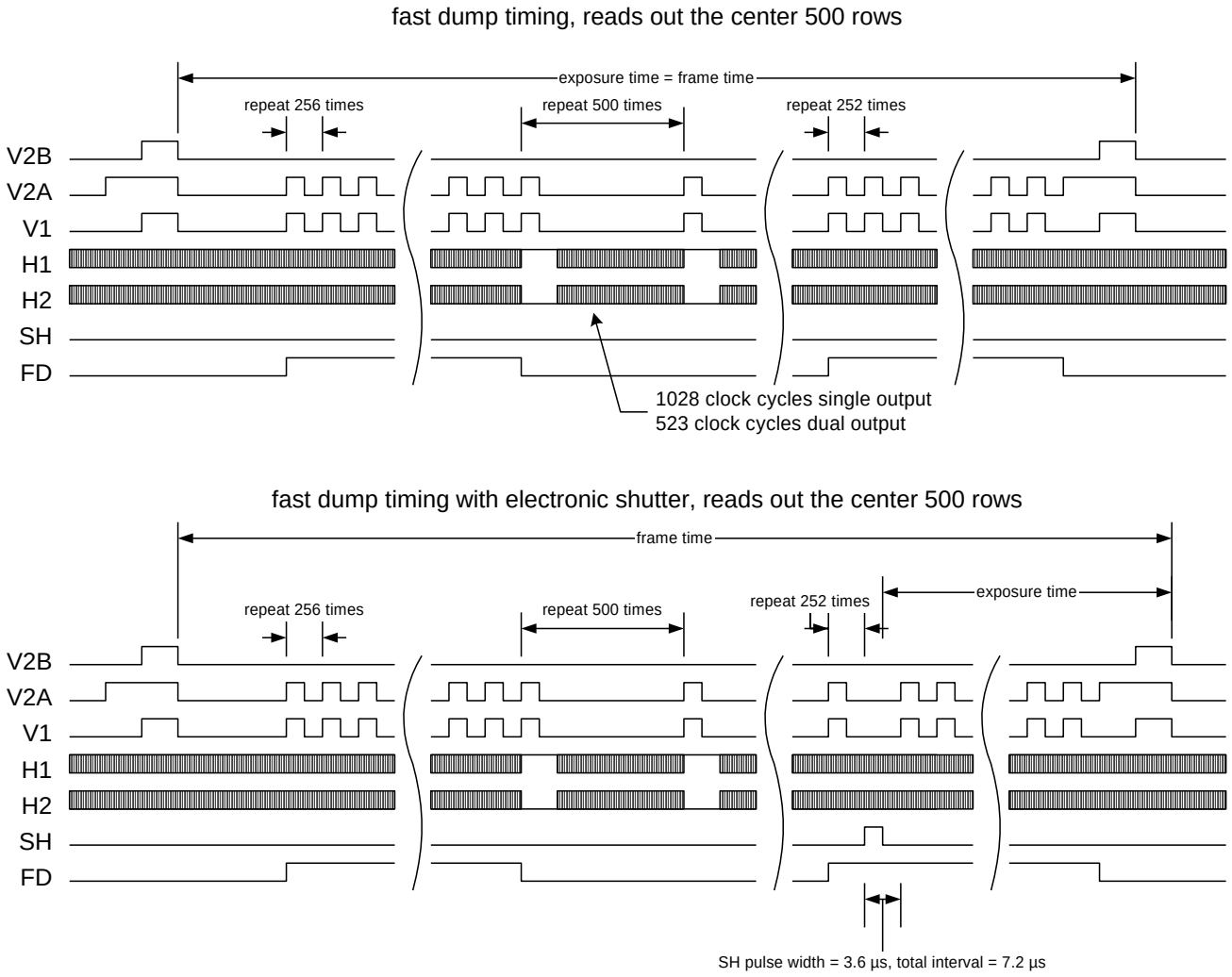


Figure 31: Interlaced - Field Integration Timing Example

Camera Design

Low Level Block Diagram

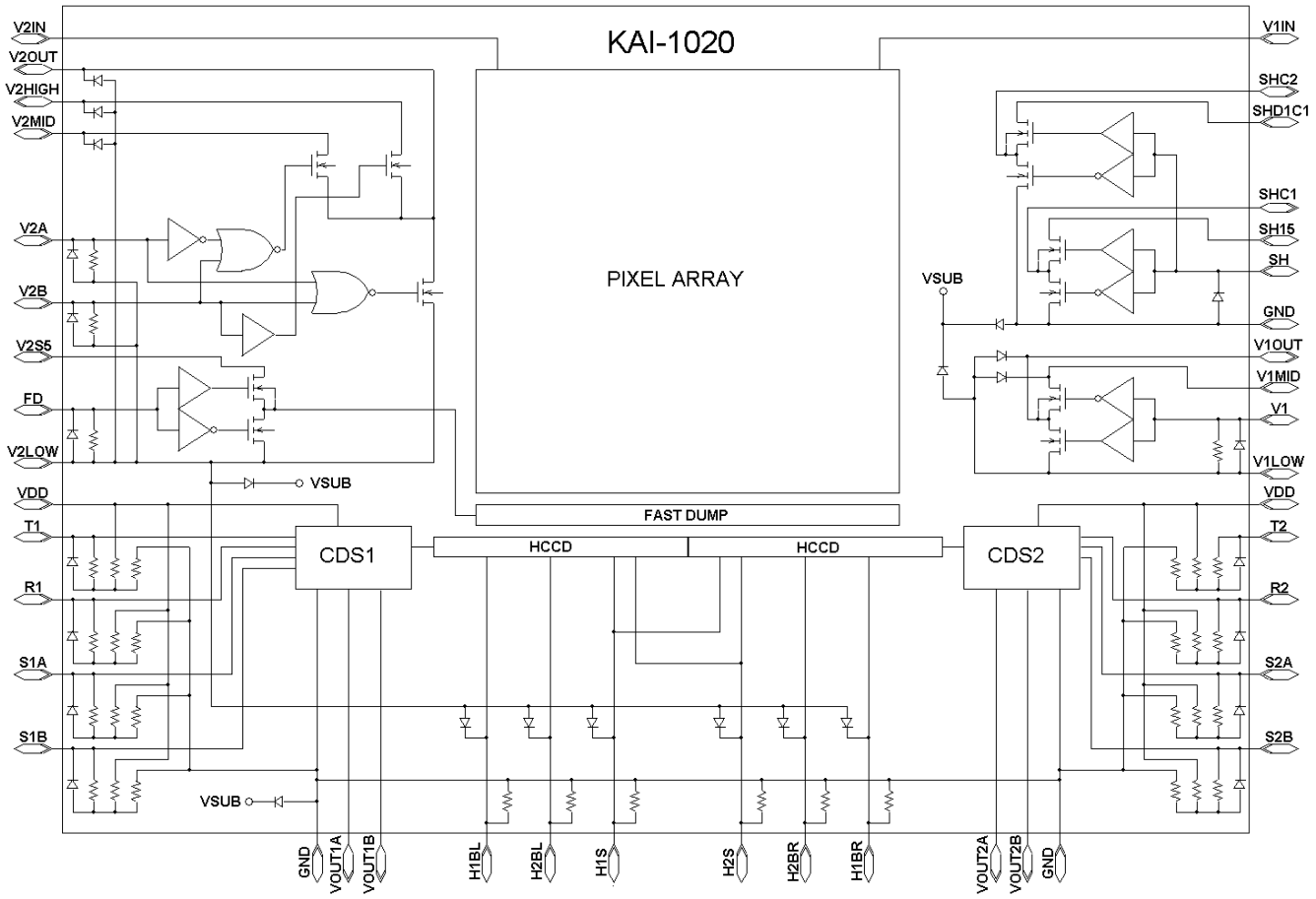


Figure 32: Low Level Block Diagram

HORIZONTAL CCD DRIVE CIRCUIT

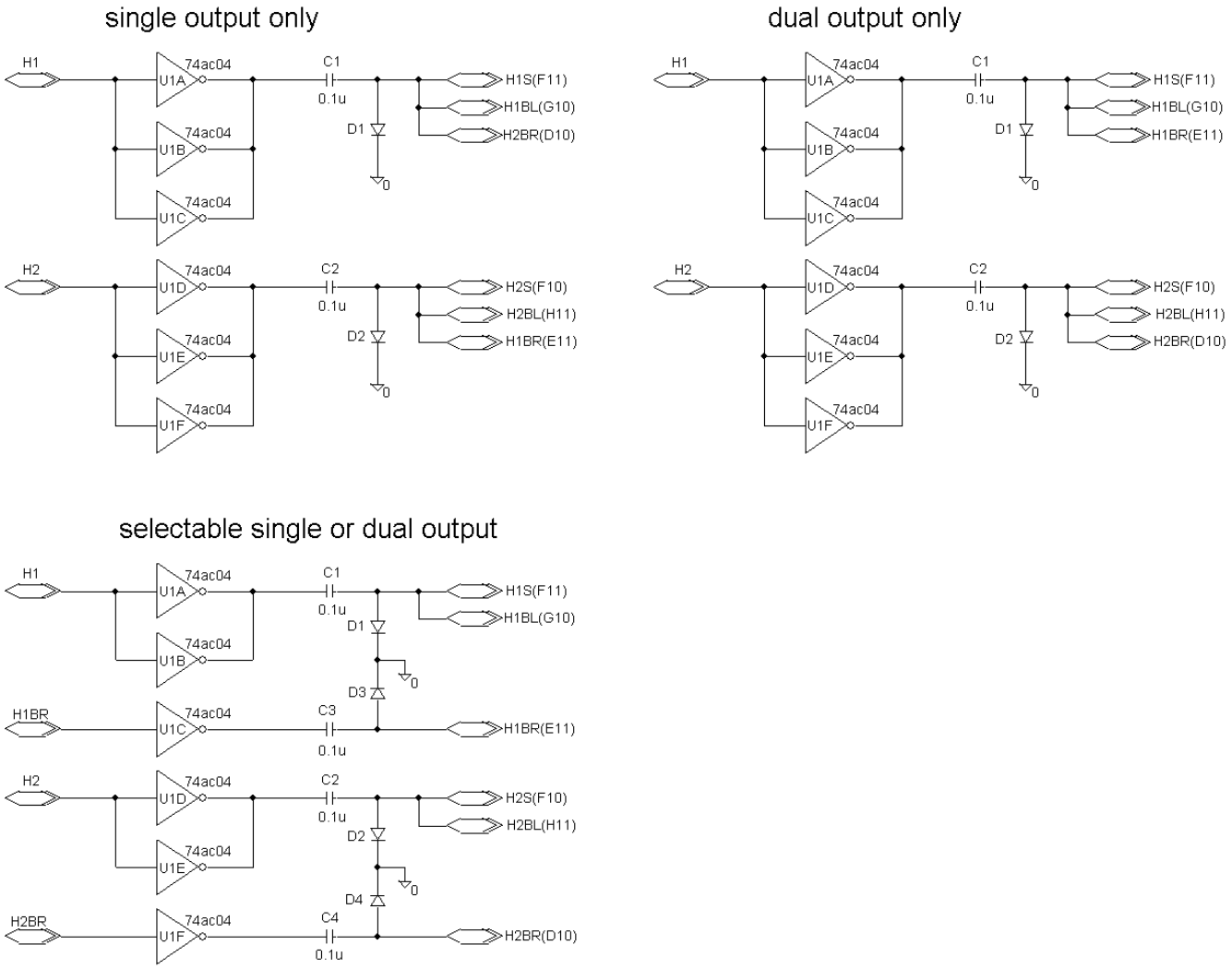


Figure 33: HCCD Drive Circuit Block Diagram

The HCCD clock inputs should be driven by buffers capable of driving a capacitance of 60 pF and having a full voltage swing of at least 4.7 V. A 74AC04 or equivalent is recommended to drive the HCCD. The HCCD requires a 0 to –5 V clock. A negative clock level is easily obtained by capacitive coupling and a diode to clamp the high level to GND. Every HCCD clock input has a 300 kΩ on chip resistor to GND.

The inputs to the above circuits, H1 and H2, are 5V logic from the timing generator (a programmable gate array for example). If the camera is to have selectable single or dual output modes of operation, then the timing logic needs to generate two extra signals for the H1BR and H2BR timing. For single output mode program the timing such that H1BR=H2 and H2BR=H1. For dual output mode program the timing such that H1BR=H1 and H2BR=H2.

VERTICAL CCD

The VCCD clock inputs, φV2A, φV2B, φV1, and φFD have a capacitive load of approximately 10 pF. Each input is connected to V2LOW and V1LOW by a 60 kΩ internal resistor. There is also an internal diode connected to V2LOW and V1LOW. The 5 V logic drivers must be connected to the sensor inputs through capacitors. These inputs require a clock of at least 4 V amplitude. Most PGA's can drive these inputs directly. The external capacitor and internal diode level shift the 0V to 5V input to V2LOW to V2LOW + 5.

The on chip VCCD clock drivers switch their outputs, V1OUT and V2OUT, between the supply voltages V1LOW, V1MID, V2LOW, V2MID, and V2HIGH. The truth table correlating the voltage on V1OUT and V2OUT to the timing inputs is:

φV1	V1OUT
L	V1MID
H	V1LOW

φV2A	φV2B	V2OUT
L	L	V2LOW
H	L	V2MID
L	H	V2HIGH
H	H	V2HIGH

L = logic low level
H = logic high level

The output of the VCCD driver is connected to the VCCD gates by wiring V1OUT to V1IN and V2OUT to V2IN. The fast dump driver has no external output. It is wired internally to the VCCD fast dump gate.

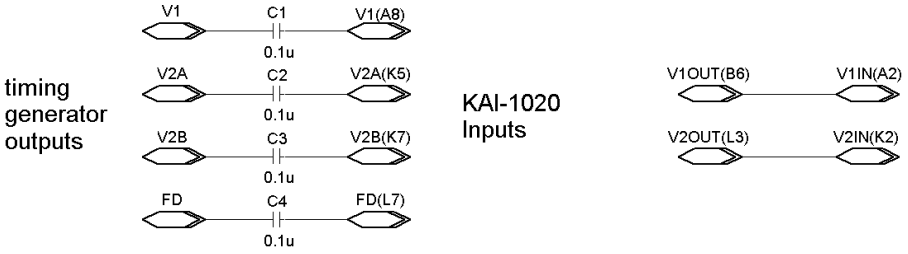


Figure 34: VCCD Block Diagram

ELECTRONIC SHUTTER

The electronic shutter input, φSH, is the only input driven directly by CMOS logic. No capacitive coupling is required. φSH (pin B3) has approximately a 10 pF load. The logic low level must be less than 0.5 V and the logic high level must be greater than 3.5 V. Most programmable gate arrays can drive φSH directly. The on chip electronic shutter driver is a charge pumping circuit. It uses C1, C2, D1, and D2 to generate a >25 V pulse that is added onto the substrate DC bias voltage. The substrate bias voltage is set by a trim-pot R2 or by some programmable voltage source. The substrate bias voltage absolutely MUST be adjustable. The camera designer CAN NOT rely on every KAI-1020 image sensor requiring the same substrate bias. An adjustment range of 8 to 13 V must be allowed. Each image sensor has the optimal substrate bias voltage (as measured on the VSUB pin) printed on the shipping container.

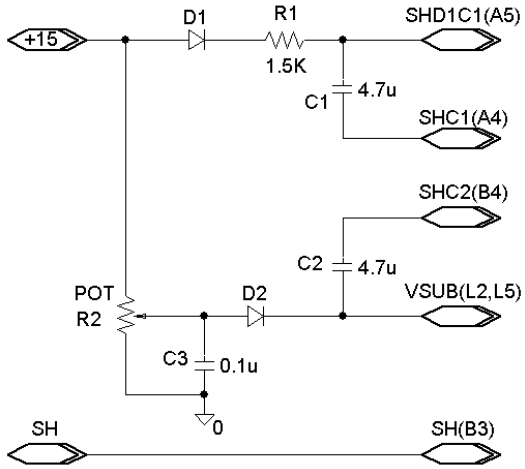


Figure 35: Electronic Shutter Block Diagram

The minimum allowed voltage on VSUB is 8 V. Lower voltages may destroy the CDS and clock driver circuits.

Note: Extremely bright light can potentially harm solid state imagers such as Charge-Coupled Devices (CCDs). Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions*.

CDS Timing Inputs

The CDS timing inputs φR, φT, φSA, and φSB should be driven by CMOS logic with fast rise and fall times and an amplitude of at least 4.7 V. The capacitance of each pin on the sensor is approximately 10 pF. The pulses are level shifted positive by 1 V or 2 V on the sensor. If driving this input directly from a programmable gate array, be aware that some PGA's do not have outputs with amplitudes of 4.7 V. It is recommended that the CDS timing inputs be driven by a 74AC04 to insure a 5 V pulse amplitude with fast edges.

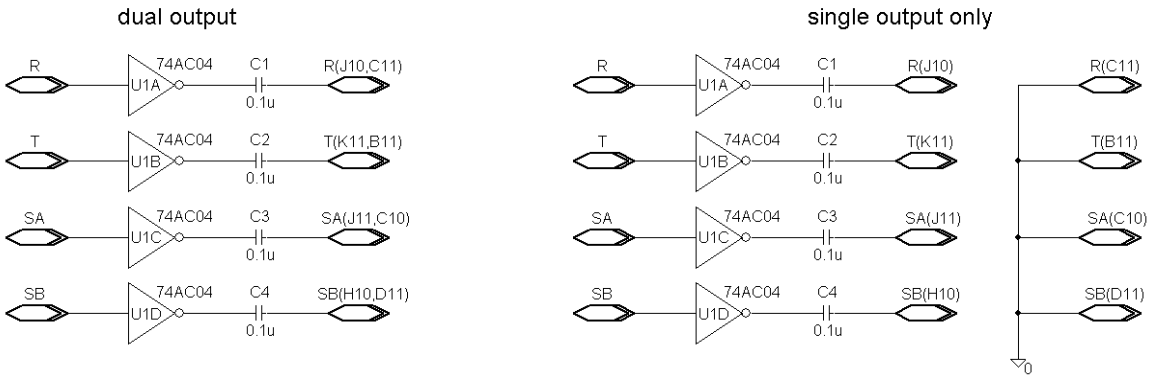


Figure 36: Correlated Double Sampling Block Diagram

If the camera will only operate in single output mode then the φR2, φT2, φS2A, and φS2B inputs should be connected to GND. All CDS timing inputs must be coupled with a capacitor.

CDS Output Circuit

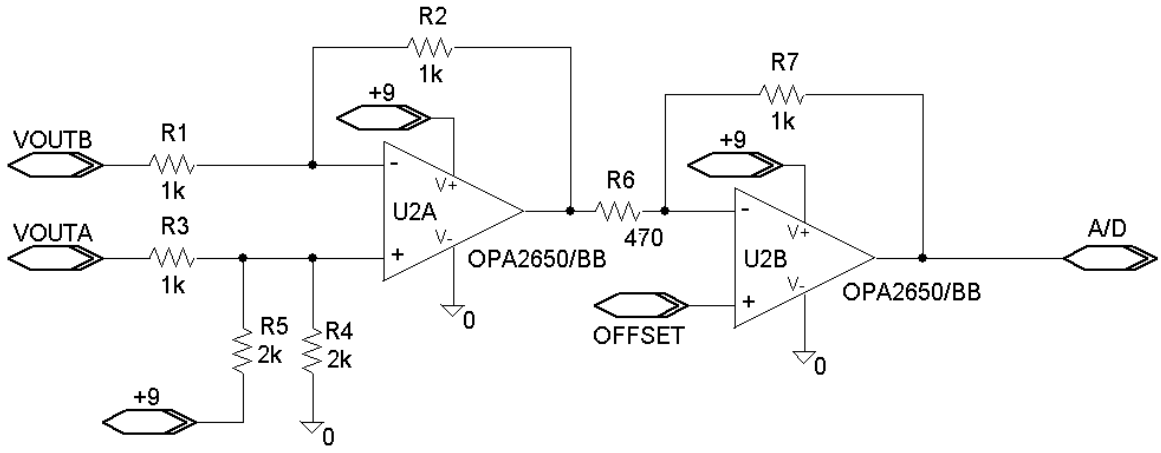


Figure 37: Correlated Double Sampling Output Circuit Block Diagram

In the above schematic the differential video outputs VOUTB and VOUTA are subtracted by op-amp U2A. The video outputs will have a DC level of 7 to 11 V. U2B then inverts the signal and applies a gain of 2.1 relative to the offset voltage. The output of U2B will match the 500 mV output range of the KAI-1020 to the 1 V input range of the analog to digital converter (A/D).

VOUTB will swing in the negative direction with increasing light level. The output of U2A will swing in the positive direction with increasing light level. The output of U2B (input to the A/D) will swing in the negative direction. This means the A/D output will be 0 counts when the image sensor is saturated. The digital data will have to be inverted before being transmitted to a digital image capture device. See the KAI-1020 evaluation board schematic for a simple method of inverting the data with no additional components.

The offset will have to be dynamically adjusted to match the zero light level of the image sensor. A circuit should examine the digital data in the dark reference columns and adjust the offset voltage of U2B to maintain a constant zero reference level in the A/D converter. The dynamic adjustment of the offset voltage will remove most temperature dependent drifts. Small temperature-dependent gain changes will still be present. See the KAI-1020 evaluation board schematic for an example of a circuit to generate the offset voltage.

This output circuit provides 10 bits of dynamic range on the KAI-1020 evaluation board. It is not the optimum circuit. For optimum differential common mode noise rejection and linearity, the CDS output circuit should take into account the 160 Ω impedance of the CDS output drive transistor.

POWER SUPPLIES

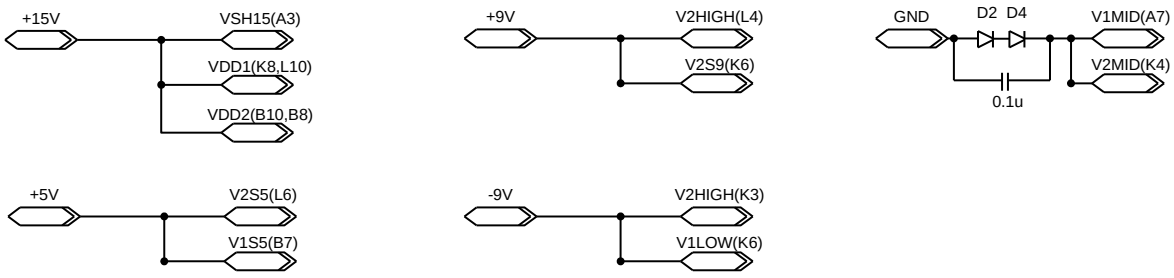


Figure 38: Power Supply Block Diagram

The V1MID and V2MID connections must be set to –1.0 to –1.5 V. Since V1MID and V2MID only sink current, two diodes can be used to set this voltage.

If the sensor is to use only the single output mode, then VDD2(B10,B8) can be connected to GND. VOUT2A(A9) and VOUT2B(A10) also should be connected to GND in the single output only mode.

KAI-1020 Evaluation Board

Front Side

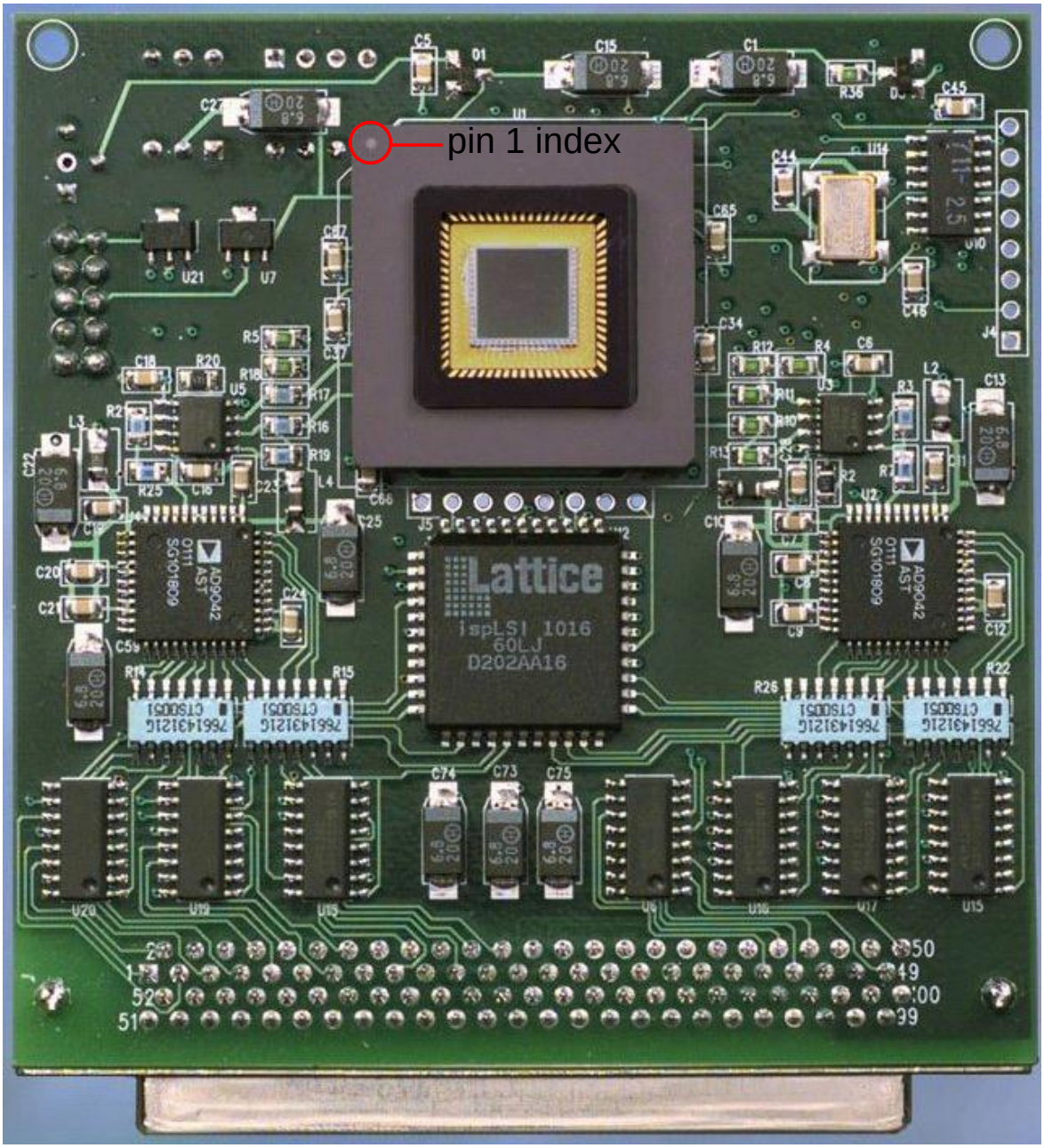


Figure 39: Evaluation Board - Front Side

Back Side

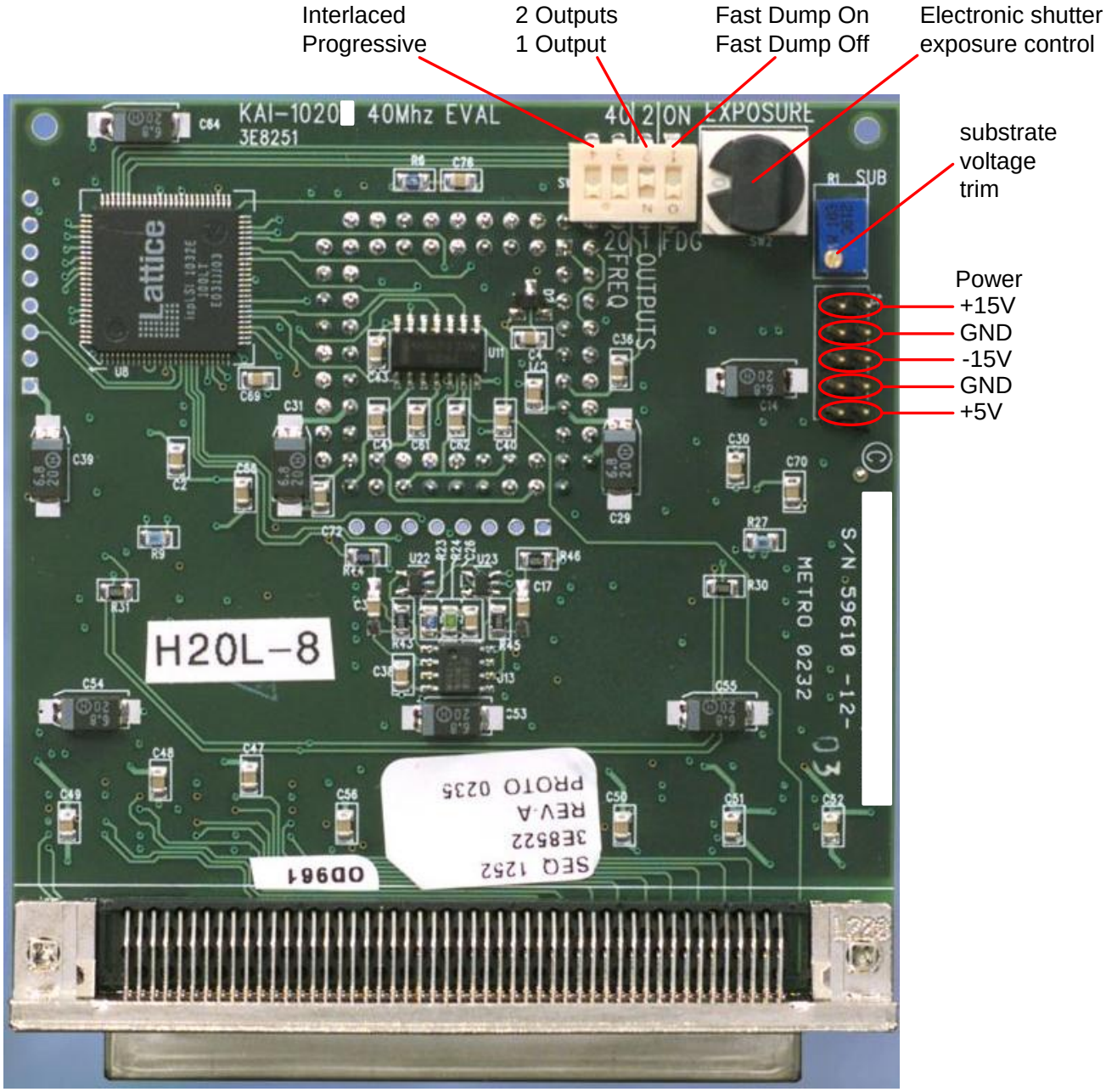


Figure 40: Evaluation Board - Back Side

SCHEMATICS

KAI-1020

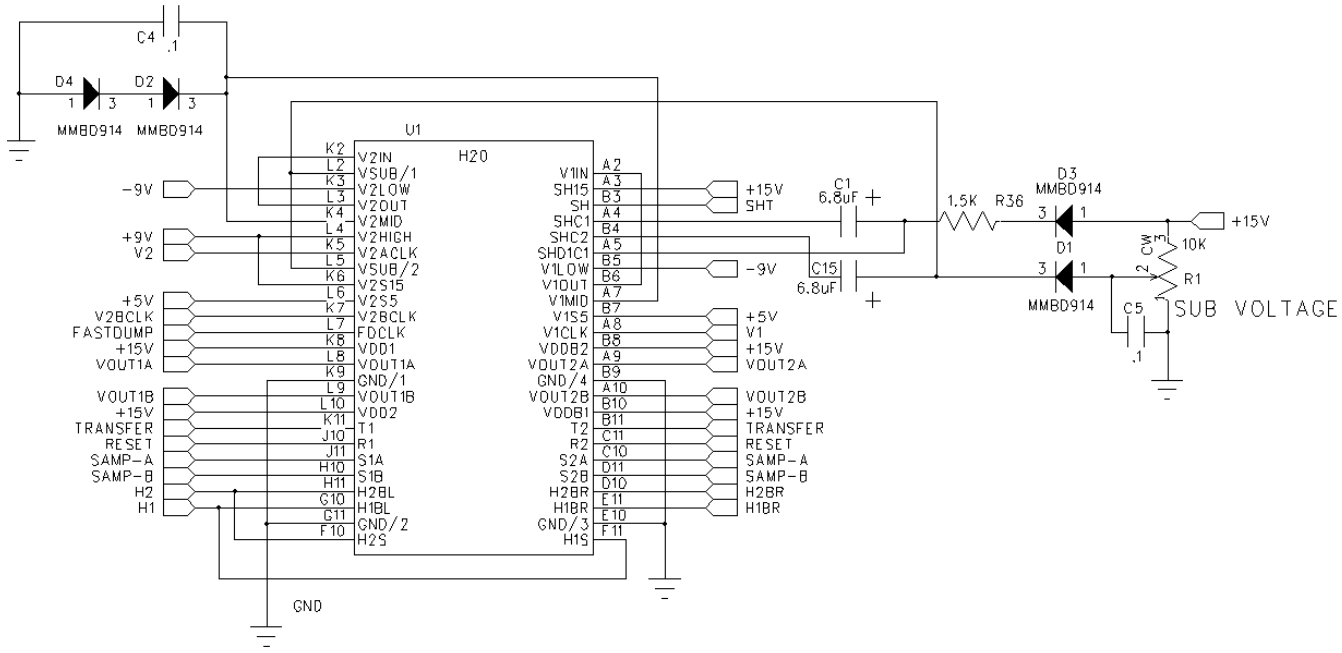


Figure 41: KAI-1020 Schematic

Timing Logic

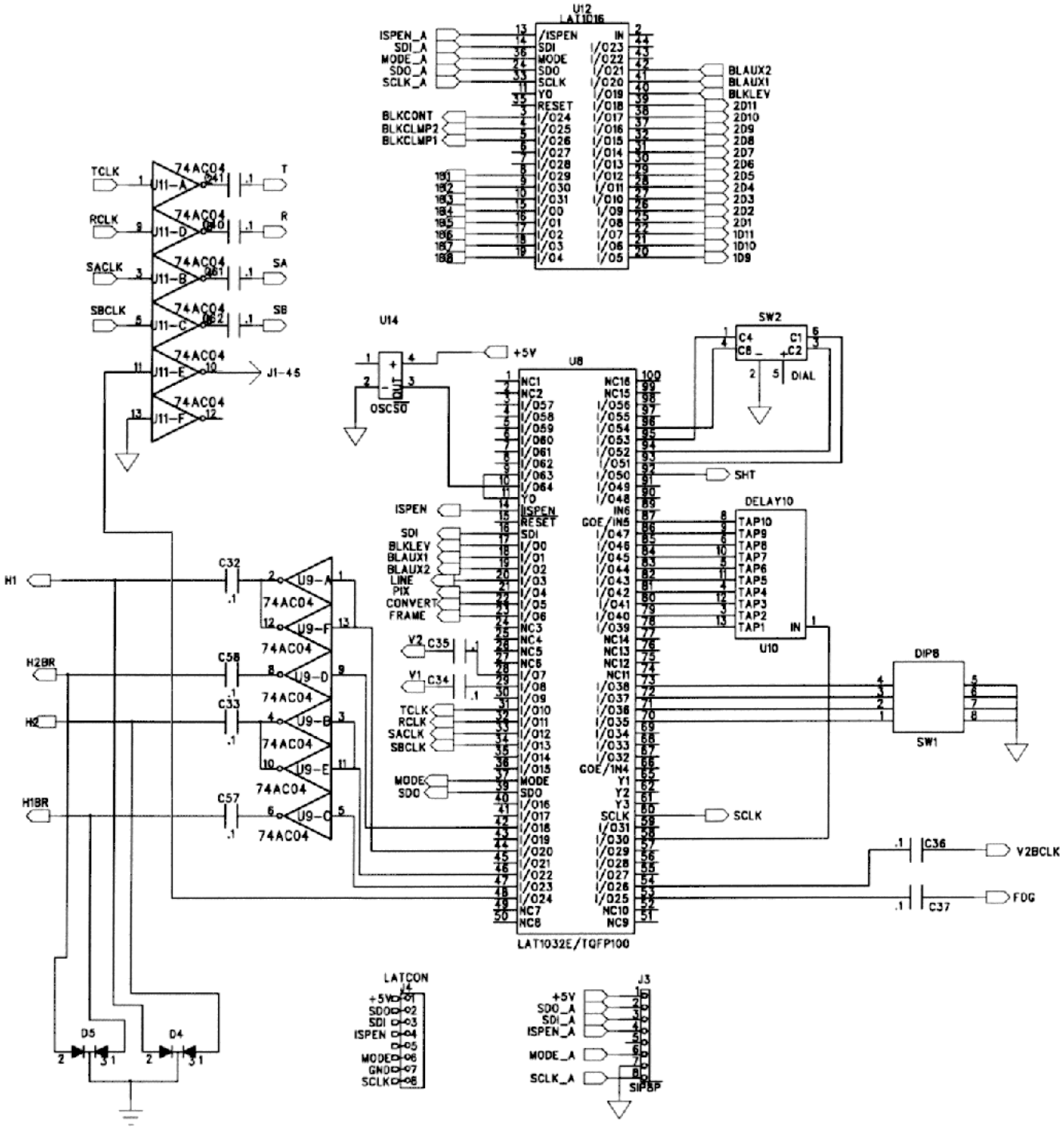


Figure 42: Timing Logic Schematic

Output 1

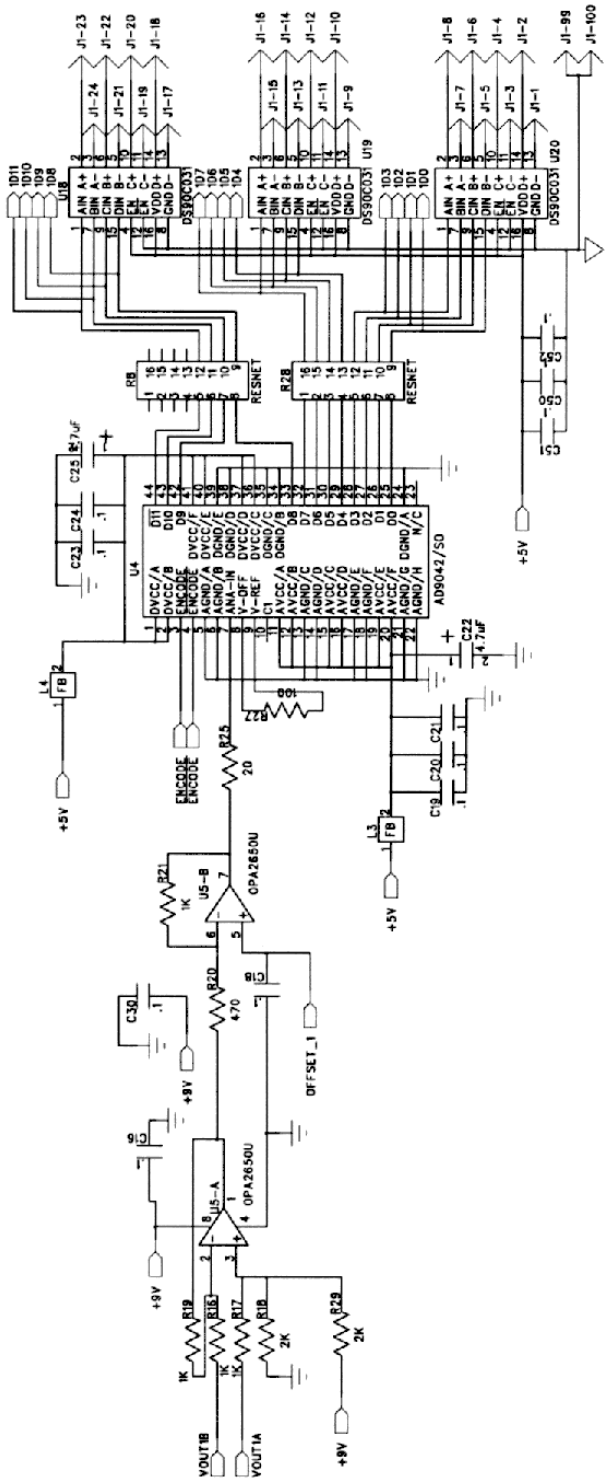


Figure 43: Output 1 Schematic

Output 2

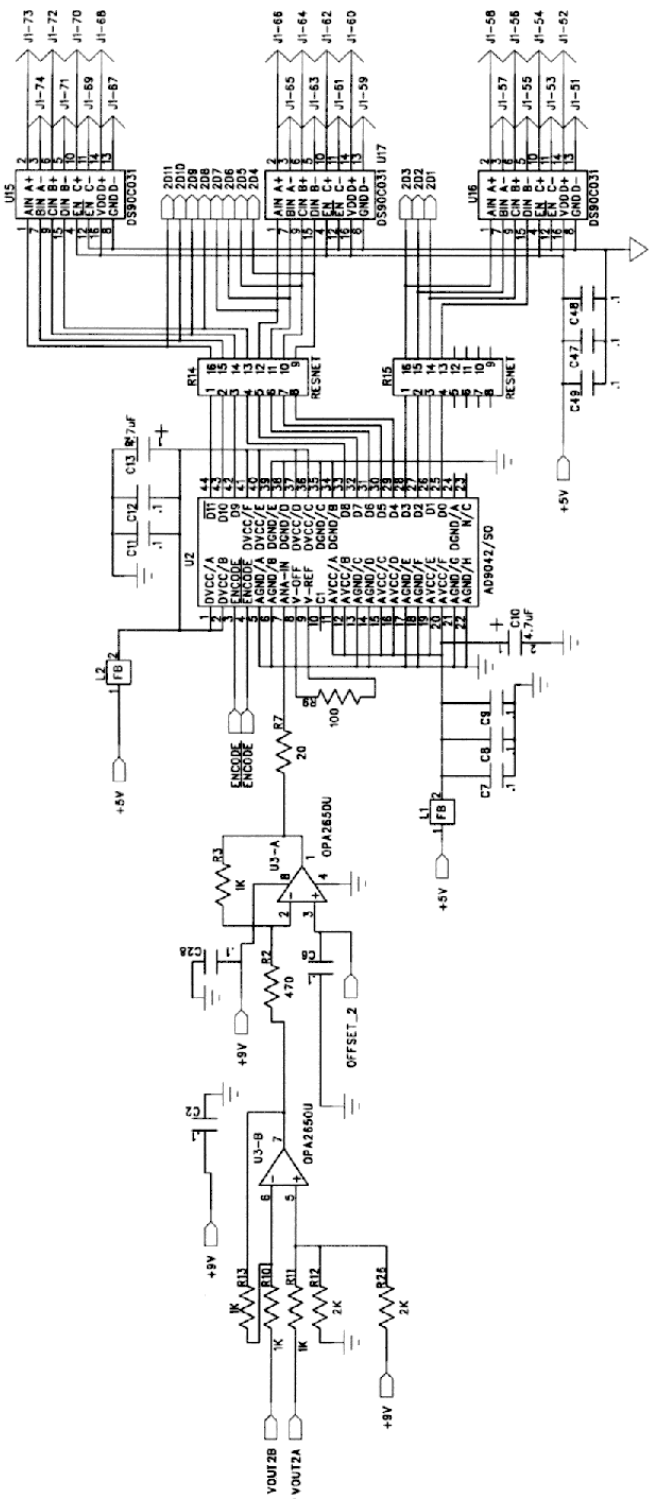


Figure 44: Output 2 Schematic

Automatic Offset and Power Supply

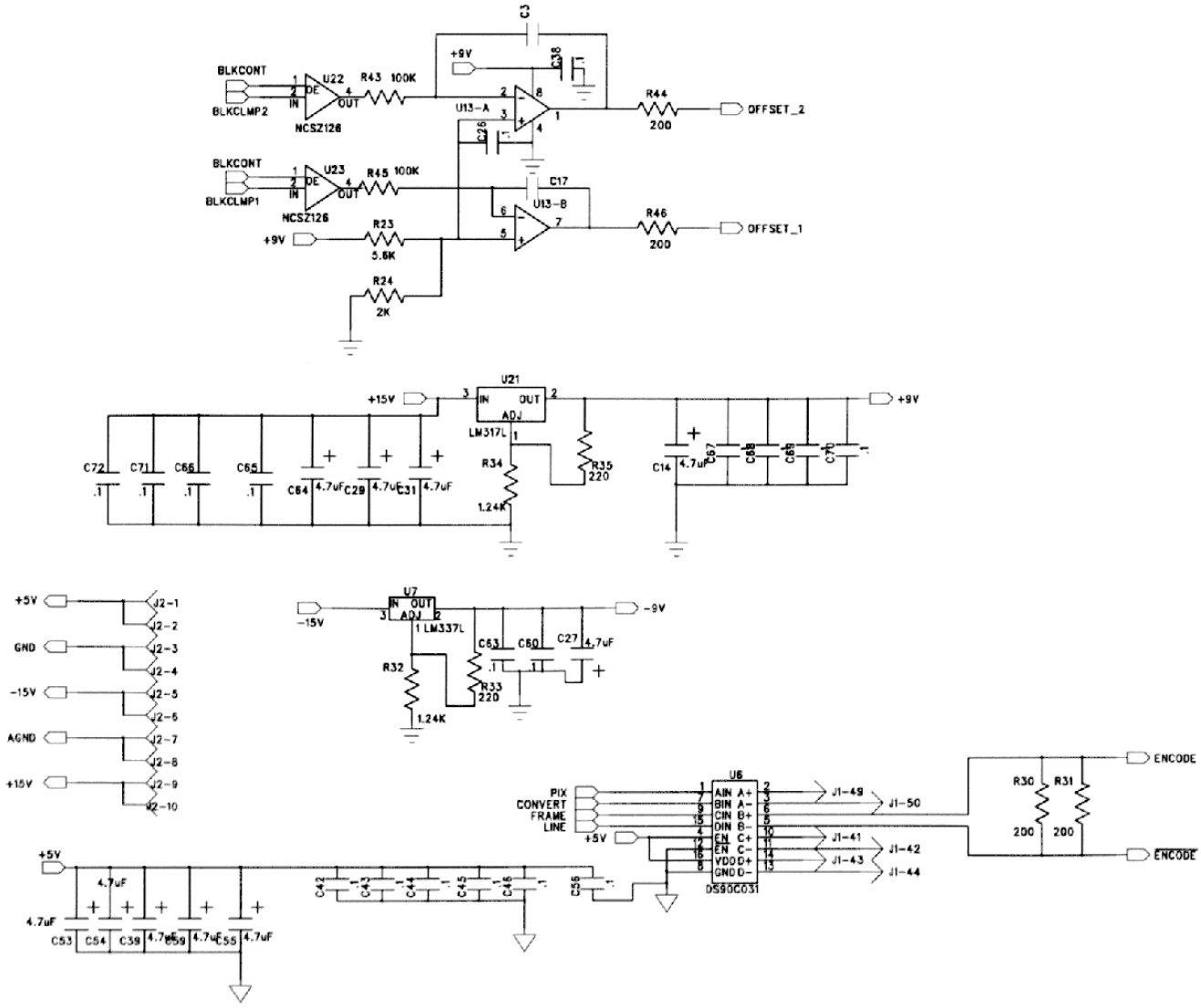


Figure 45: Automatic Offset and Power Supply Schematic

PARTS LIST

C1	PCAP, 4.7µF
C2	CAP, 0.1µF
C3	CAP, 1µF
C4-9	CAP, 0.1µF
C10	CAP, 4.7µF
C11, C12	CAP, 0.1µF
C13-15	CAP, 4.7µF
C16	CAP, 0.1µF
C17	CAP, 1µF
C18-21	CAP, 0.1µF
C22	CAP, 4.7µF
C23, C24	CAP, 0.1µF
C25	CAP, 4.7µF
C26	CAP, 0.1µF
C27	CAP, 4.7µF
C28	CAP, 0.1µF
C29	CAP, 4.7µF
C30	CAP, 0.1µF
C31	CAP, 4.7µF
C32-38	CAP, 0.1µF
C39	CAP, 4.7µF
C40-52	CAP, 0.1µF
C53-55	CAP, 4.7µF
C56-58	CAP, 0.1µF
C59	CAP, 4.7µF
C60-63	CAP, 0.1µF
C64	CAP, 4.7µF
C65-72	CAP, 0.1µF
D1-3	MMBD914
D4, D5	MMBD2837

R1	VRES,10K
R2	RES,470
R3	RES,1K
R7	RES,20
R8	RESNET
R9	RES,100
R10, R11	RES,1K
R12	RES,2K
R13	RES,1K
R14	RESNET
R15	RESNET
R16, R17	RES,1K
R18	RES,2K
R19	RES,1K
R20	RES,470
R21	RES,1K
R23	RES,5.6K
R24	RES,2K
R25	RES,20
R26	RES,2K
R27	RES,100
R28	RESNET
R29	RES,2K
R30	RES,200
R31	RES,200
R32	RES,1.24K
R33	RES,220
R34	RES,1.24K
R35	RES,220
R36	RES,1.5K
R43	RES,100K
R44	RES,200
R45	RES,100K
R46	RES,200

SW1	DIP8	4 POS DIP SW
SW2	DIAL	16 POS ROTARY
U1	KAI1020	IMAGE SENSOR
U2	AD9042/SO	A/D ANALOG DEV
U3	OPAMP DUAL,OPA2650U	BURR BROWN
U4	AD9042/SO	A/D ANALOG DEV
U5	OPAMP DUAL,OPA2650U	BURR BROWN
U6	DS90C031	NATIONAL
U7	LM337L	
U8	LAT1032E TQFP100	LATTICE SEMI
U9	74AC04	
U10	DELAY10	DATA DELAY DEV 711 2.5 ns
U11	74AC04	
U12	LAT1016	LATTICE SEMI
U13	OPAMP-DUAL, LMC6492BEM	NATIONAL
U14	OSC\SO	80 MHZ
U15-20	DS90C031	NATIONAL
U21	LM317L	
U22, U23	NC7SZ126	FAIRCHILD
L1-4	FB	FERRITE BEAD
J1	SCSI-100	
J2	HEADER10	POWER CONN
J3	SIP\8P	PROGRAM CONN
J4	LATCON	PROGRAM CONN

DIGITAL OUTPUT CONNECTOR

The output connector is a 100 pin female SCSI type connector, pin compatible with the National Instruments PCI-1424 digital frame grabber, part number 777662-02. The interface cable is available from National Instruments, part number 185012-02.

Output 1	Pin
data 0+	1
data 0-	2
data 1+	3
data 1-	4
data 2+	5
data 2-	6
data 3+	7
data 3-	8
data 4+	9
data 4-	10
data 5+	11
data 5-	12
data 6+	13
data 6-	14
data 7+	15
data 7-	16
data 8+	17
data 8-	18
data 9+	19
data 9-	20
data 10+	21
data 10-	22
data 11+	23
data 11-	24

Output 2	Pin
data 0+	51
data 0-	52
data 1+	53
data 1-	54
data 2+	55
data 2-	56
data 3+	57
data 3-	58
data 4+	59
data 4-	60
data 5+	61
data 5-	62
data 6+	63
data 6-	64
data 7+	65
data 7-	66
data 8+	67
data 8-	68
data 9+	69
data 9-	70
data 10+	71
data 10-	72
data 11+	73
data 11-	74

Sync	Pin
pixel +	49
pixel -	50
line +	43
line -	44
frame +	41
frame -	42
field index	45
GND	99
GND	100

All other pins have no connection. All outputs are driven by low voltage differential line drivers (LVDS) except for the field index which is TTL.

Power Connector

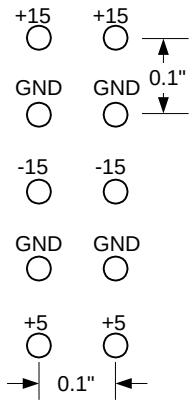


Figure 46: Power Connector Block Diagram

The evaluation board requires +15 V, -15 V, and +5 V. The current draw for each supply is:

Supply	Current (mA)
+15	62
-15	18
+5	780

Mode Switch

Switch	On	Off
1	Fast Dump off	Fast Dump on
2	1 output	2 outputs
3	---	----
4	Progressive scan	Interlaced

When the fast dump is activated the timing dumps the first 256 lines, then reads out 512 lines of image data, and finally it dumps the last 240 lines. The resulting image is 1000 columns by 512 rows. The interlaced mode timing is not programmed to support fast dumping.

Exposure Switch

All exposure times are in µs. Electronic shuttering is not programmed into the timing generator for interlaced mode.

Exposure Setting	FD Off: 1 output	FD Off: 2 outputs	FD On: 1 output	FD On: 2 outputs
0	33300	20600	20600	14160
1	16400	10160	6000	4400
2	7960	4960	3000	2540
3	3740	2320	1860	1840
4	1616	1016	1700	1700
5	564	362	824	824
6	298	198	460	460
7	68	55	93	93

Substrate Voltage Trim

This variable resistor allows the substrate voltage to be varied from 0 V to 15 V. Adjusting this voltage will change the charge capacity and anti-blooming of the pixel photodiodes. Do not adjust the voltage below 8 V.

Evaluation Board Notes

Timing

The main timing is generated by a programmable gate array U8. The HCCD drive is setup for selectable single or dual output by inverting the H2BR and H2BL timing signals depending on the setting of the mode switch SW1.

The short pulses for φR, φT, φSA, and φSB are generated by combining (logical and/or) the outputs of the delay line U10. Each tap on U10 delays the system clock by 2.5ns.

The amount of noise in the KAI-1020 will have a strong dependence on the stability of the timing inputs. The most sensitive inputs are the HCCD and the CDS timing inputs. The evaluation board uses one PGA (U8) to hold all of the counters and to generate the CDS timing. This is not the optimum arrangement. Though gray code counters were used, some fixed pattern column noise can be seen in the image from the counters inside U8. The counters inside U8 cause small disturbances of the HCCD and CDS timing. One solution to eliminate this noise source is to separate the counters and CDS pulse generation into two separate PGA's. One PGA would contain all of the counters for the rows and columns, and send a HCCD gating signal to a second PGA. The second PGA would output the HCCD clock as well as form the CDS timing pulses from the multi-tap delay line U10. This second PGA would contain no counters.

Output Channel

The output circuit is identical to section 0. The two op-amps U5A and U5B present an inverted signal to the ADC U4. The offset circuit will maintain the digital output of U4 at 4080 when the image sensor is in the dark. The output of U4 will be zero when the image sensor is saturated with light. The digital data is inverted by swapping the high and low outputs of the differential line drivers on the output connector.

Automatic Offset

U12 is used to control the automatic offset circuit. U8 sends a signal to U12 on the line BLKLEV when the output of the analog to digital converter corresponds to the center 10 columns of the KAI1020 dark reference. When U12 receives the signal from U8, U12 compares the outputs of the A/D converters to the number 4080. If the output is above or below 4080, U12 enables the buffers U22 and U23 and sets their inputs to cause the integrators U13A and U13B to raise or lower the offset voltages.

A separate PGA (U12) is used to monitor the output of the A/D converters. This function should not be combined with U8 into one PGA. If only one PGA is used then the digital data will cause noise in the timing outputs to the image sensor. This is especially true when the A/D outputs are near a major bit boundary, such as 2048 or 1024. At these bit boundaries there are a large number of bits changing value that would disturb the stability of the HCCD and CDS clocking.

The automatic offset updates the offset every line. This does cause some noise in the image because the offset changes slightly each line time. An improved offset circuit would measure the offset error along the entire column and then correct the offset voltage once per frame.

OSCILLOSCOPE TRACES

This section contains oscilloscope traces of signals measured on the KAI-1020 pins. Some of the timing signals are not 0 to 5V because the KAI-1020 has level shifted the signals. All signals were measured on the KAI-1020 evaluation board.

CDS Timing

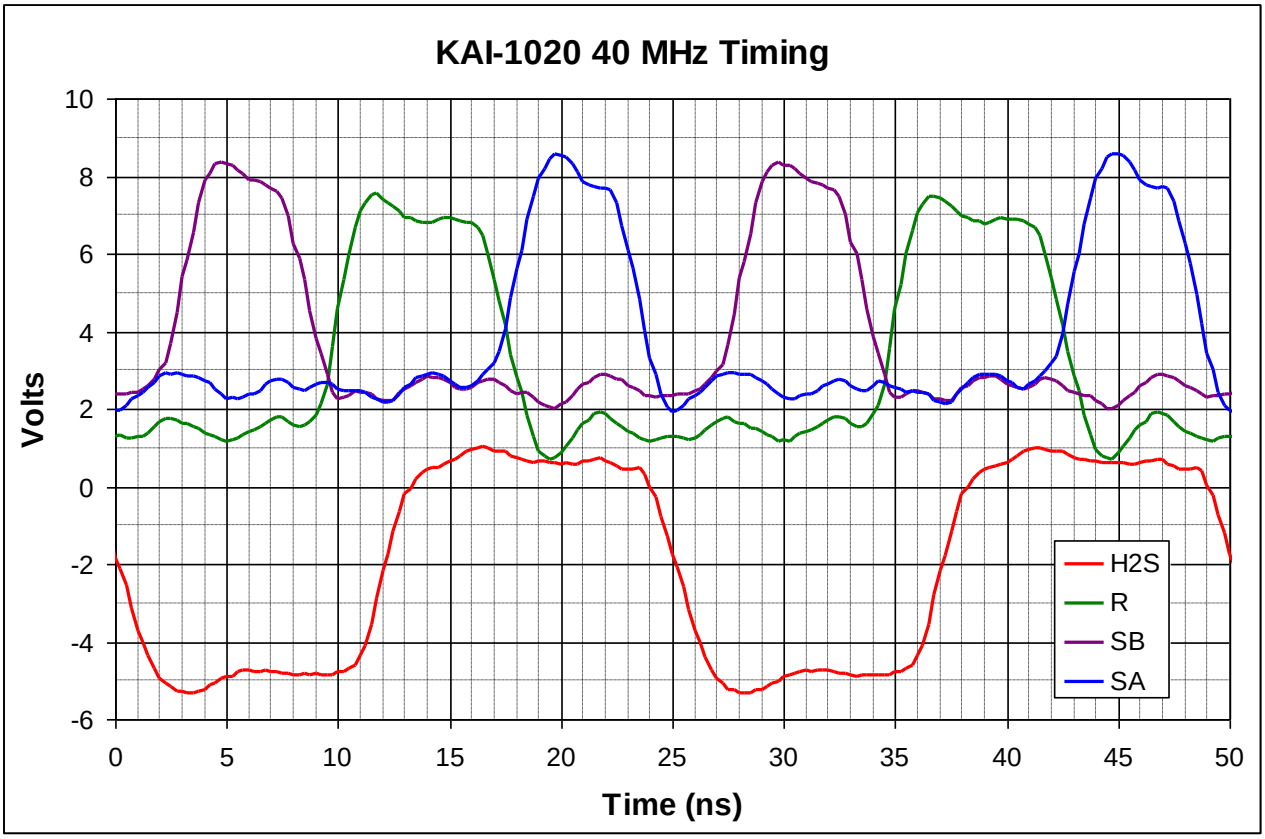


Figure 47: CDS Timing Oscilloscope Traces

Vertical Retrace

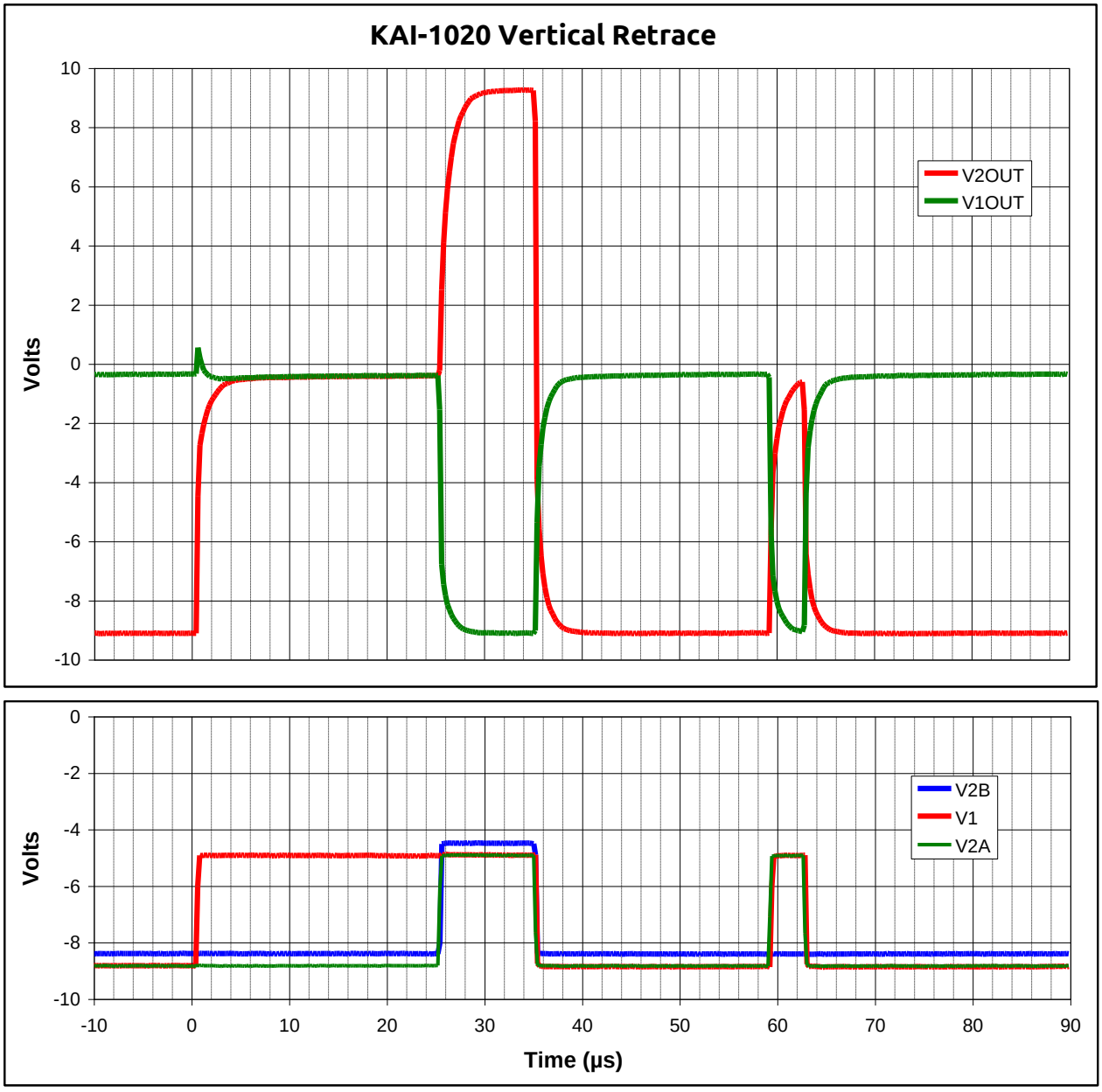


Figure 48: Vertical Retrace Oscilloscope Traces

Horizontal Retrace

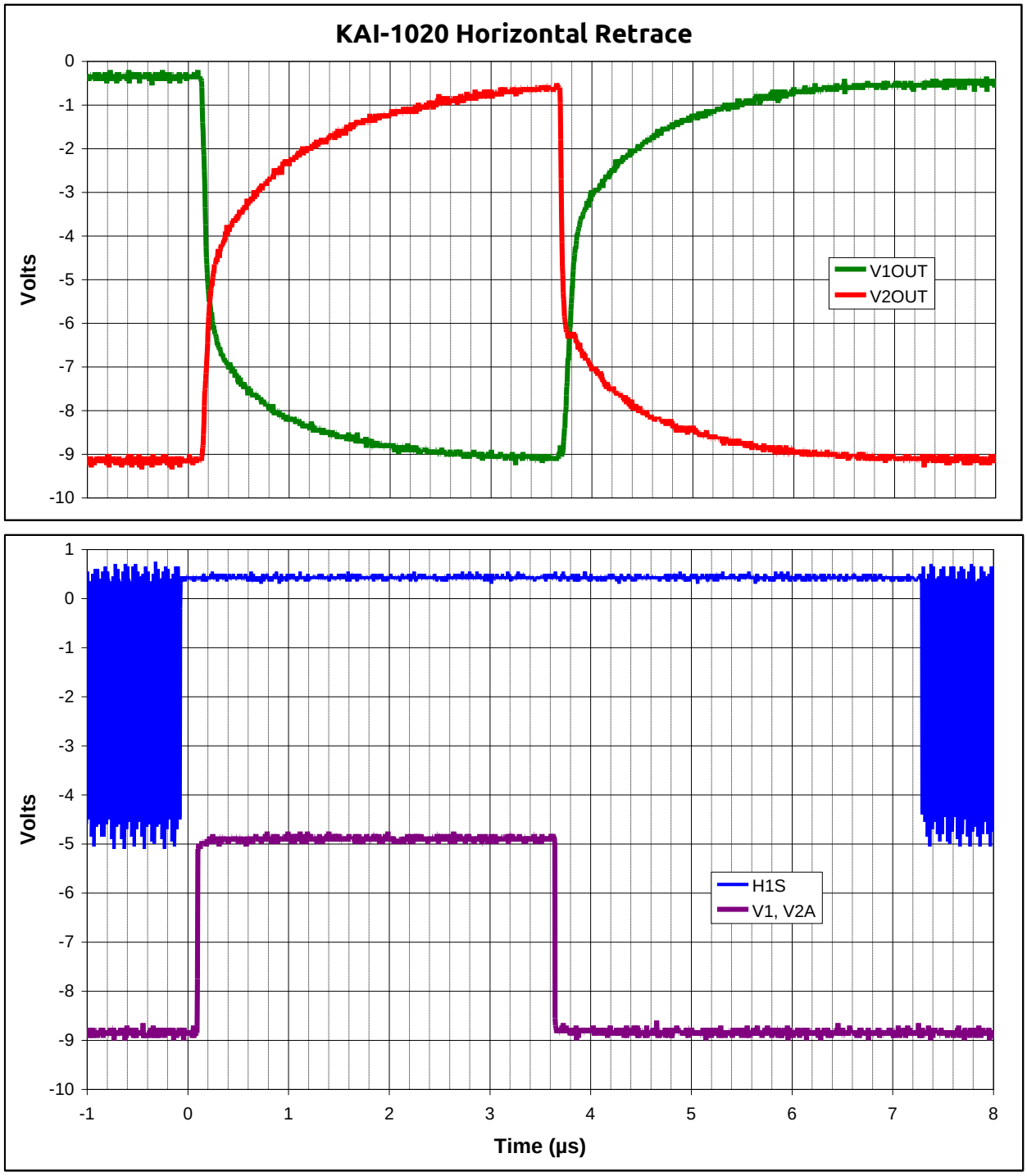


Figure 49: Horizontal Retrace Oscilloscope Traces

Storage and Handling

Storage Conditions

Description	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	T_{ST}	-55	70	°C	1
Humidity	RH	5	90	%	2

Notes:
1. Long-term exposure toward the maximum temperature will accelerate color filter degradation.
2. T=25 °C. Excessive humidity will degrade MTTF

ESD

1. This device contains limited protection against Electrostatic Discharge (ESD). ESD events may cause irreparable damage to a CCD image sensor either immediately or well after the ESD event occurred. Failure to protect the sensor from electrostatic discharge may affect device performance and reliability.
2. Devices should be handled in accordance with strict ESD procedures for Class 0 (<250V per JESD22 Human Body Model test), or Class A (<200V JESD22 Machine Model test) devices. Devices are shipped in static-safe containers and should only be handled at static-safe workstations.
3. See Application Note *Image Sensor Handling Best Practices* for proper handling and grounding procedures. This application note also contains workplace recommendations to minimize electrostatic discharge.
4. Store devices in containers made of electro-conductive materials.

Cover Glass Care and Cleanliness

1. The cover glass is highly susceptible to particles and other contamination. Perform all assembly operations in a clean environment.
2. Touching the cover glass must be avoided.
3. Improper cleaning of the cover glass may damage these devices. Refer to Application Note *Image Sensor Handling Best Practices*.

Environmental Exposure

1. Extremely bright light can potentially harm CCD image sensors. Do not expose to strong sunlight for long periods of time, as the color filters and/or microlenses may become discolored. In addition, long time exposures to a static high contrast scene should be avoided. Localized changes in response may occur from color filter/microlens aging. For Interline devices, refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible lighting Conditions*.
2. Exposure to temperatures exceeding maximum specified levels should be avoided for storage and operation, as device performance and reliability may be affected.
3. Avoid sudden temperature changes.
4. Exposure to excessive humidity may affect device characteristics and may alter device performance and reliability, and therefore should be avoided.
5. Avoid storage of the product in the presence of dust or corrosive agents or gases, as deterioration of lead solderability may occur. It is advised that the solderability of the device leads be assessed after an extended period of storage, over one year.

Soldering Recommendations

1. The soldering iron tip temperature is not to exceed 370 °C. Higher temperatures may alter device performance and reliability.
2. Flow soldering method is not recommended. Solder dipping can cause damage to the glass and harm the imaging capability of the device. Recommended method is by partial heating using a grounded 30 W soldering iron. Heat each pin for less than 2 seconds duration.

Mechanical Drawings

COMPLETED ASSEMBLY

Pin Grid Array

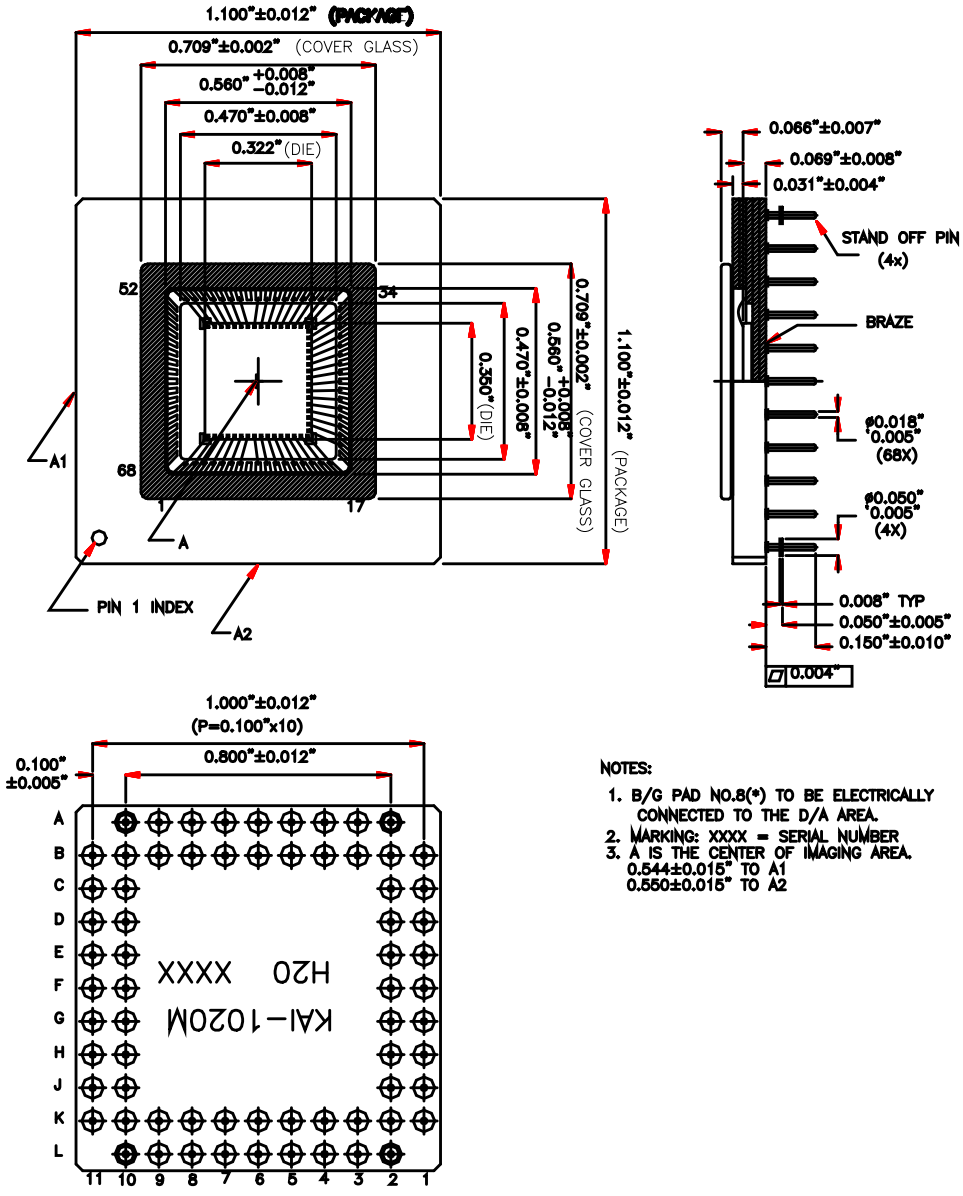


Figure 50: PGA Completed Assembly

Leadless Chip Carrier

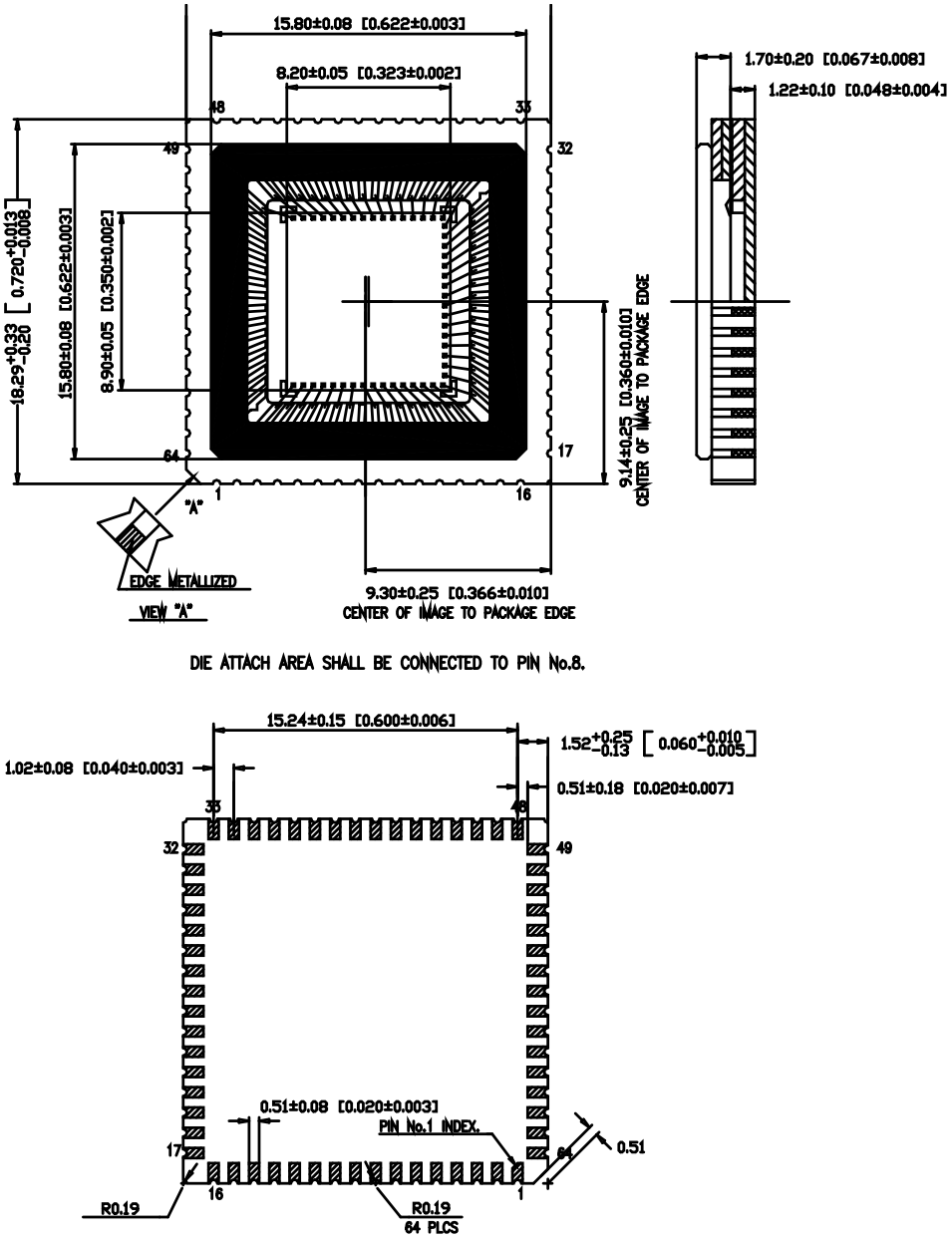


Figure 51: LCC Completed Assembly

Leadless Chip Carrier and Soldering

Care should be taken when using reflow ovens to solder the KAI-1020 to circuit boards. Extreme temperatures may cause degradation to the color filters or microlens material.

COVER GLASS

Pin Grid Array Cover Glass

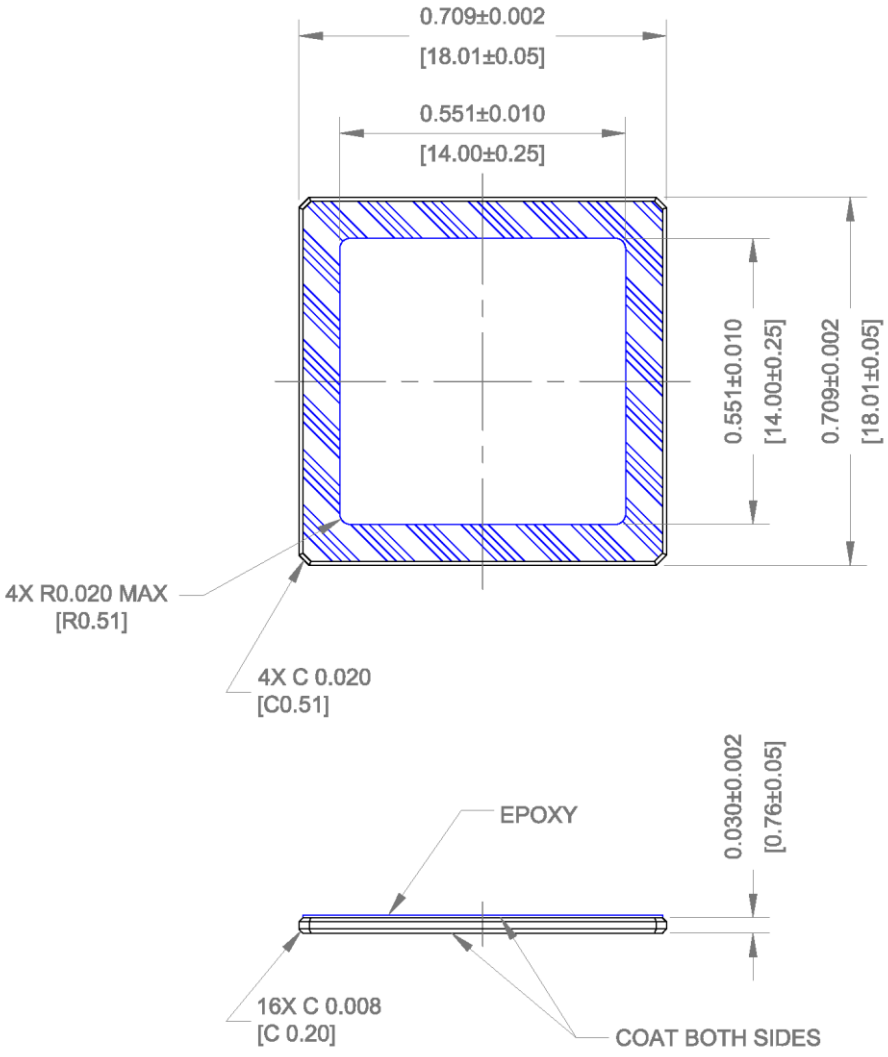


Figure 52: PGA Cover Glass

Notes:

1. Dust / Scratch 10 micron max
2. Substrate: SCHOTT D-263T eco OR Equivalent
3. Epoxy: NCO-150HB
   Thickness 0.002" – 0.005" [0.05 – 0.13]
4. Double-Sided AR Coating Reflectance
   a. 420nm – 435nm < 2.0%
   b. 435nm – 630nm < 0.8%
   c. 630nm – 680nm < 2.0%
5. Units: IN [MM]

Leadless Chip Carrier Cover Glass

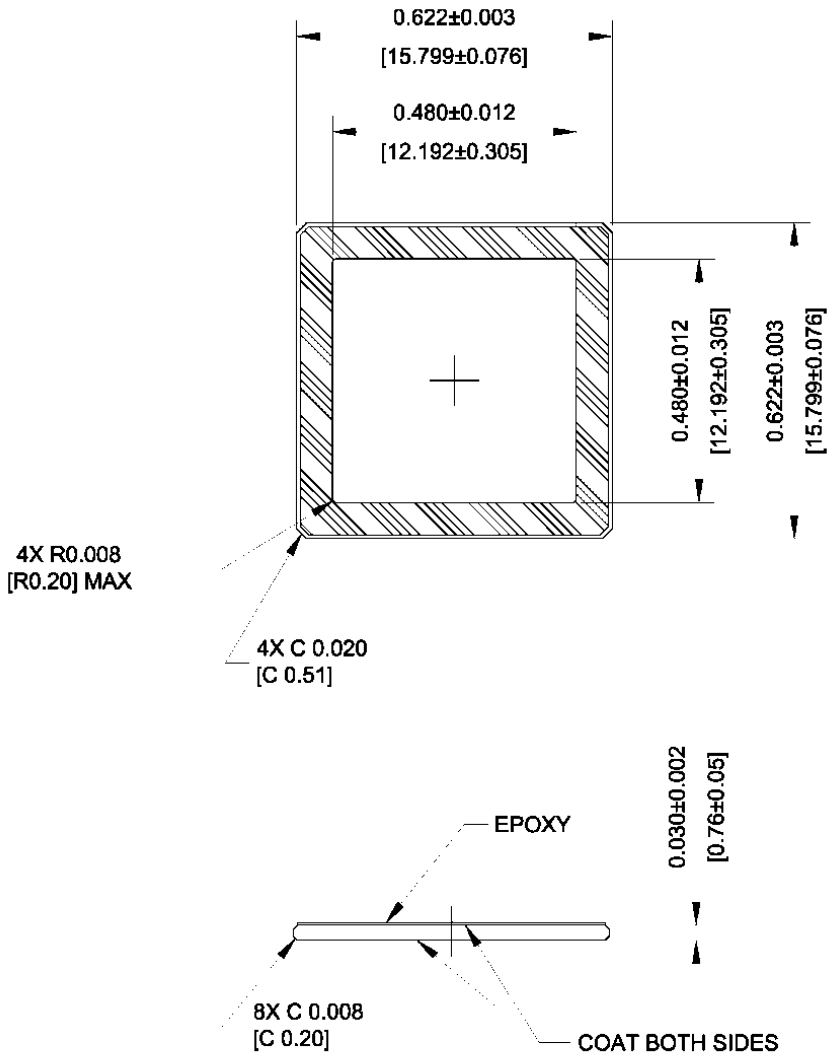


Figure 53: LCC Cover Glass

NOTE:

1. Double-side AR Coating Reflectance
   a. 420nm – 435nm < 2.0%
   b. 435nm – 630nm < 0.8%
   c. 630nm 0 680nm < 2.0%
2. Substrate: SCHOTT D-263T eco or equivalent
3. Epoxy: NCO-150HB
   Thickness 0.002” – 0.005” [0.05 – 0.13]
4. Dust, Scratch specification
   a. 10 micron max
5. UNITS: IN [MM]

Glass Transmission

Figure 54: Cover Glass Transmission

Quality Assurance and Reliability

Quality and Reliability

All image sensors conform to the specifications stated in this document. This is accomplished through a combination of statistical process control and visual inspection and electrical testing at key points of the manufacturing process, using industry standard methods. Information concerning the quality assurance and reliability testing procedures and results are available from ON Semiconductor upon request. For further information refer to Application Note *Quality and Reliability*.

Replacement

All devices are warranted against failure in accordance with the *Terms of Sale*. Devices that fail due to mechanical and electrical damage caused by the customer will not be replaced.

Liability of the Supplier

A reject is defined as an image sensor that does not meet all of the specifications in this document upon receipt by the customer. Product liability is limited to the cost of the defective item, as defined in the *Terms of Sale*.

Liability of the Customer

Damage from mishandling (scratches or breakage), electrostatic discharge (ESD), or other electrical misuse of the device beyond the stated operating or storage limits, which occurred after receipt of the sensor by the customer, shall be the responsibility of the customer.

Test Data Retention

Image sensors shall have an identifying number traceable to a test data file. Test data shall be kept for a period of 2 years after date of delivery.

Mechanical

The device assembly drawing is provided as a reference.

ON Semiconductor reserves the right to change any information contained herein without notice. All information furnished by ON Semiconductor is believed to be accurate.

Life Support Applications Policy

ON Semiconductor image sensors are not authorized for and should not be used within Life Support Systems without the specific written consent of ON Semiconductor.

Revision Changes

MTD/PS-0205

Revision Number	Description of Changes
0.0	• Original formal version.
1.0	• Correct VS29 connection to 9 volt supply, not 15 volt supply in schematic on page 42. • Added Revision Changes
2.0	• Added section 1.3.5 General – Color • Added section 1.4.2 Color Quantum Efficiency • Added section 1.4.3 Color Filter Array Pattern • Updated section 2.2.1 Pin Grid Array Package Drawing • Added section 2.2 Leadless Chip Carrier Package • Added section 3 Glass • Section 5.6 Changed "DC level of 7 to 9C" to "DC level of 7 to 11V" • Section 6.5 Parts List • U13: Corrected from OPAMP-DUAL LM 649BEM to LMC6942BEM • U22, U23: Corrected from NCSZ126 to NC7SZ126
3.0	• Updated page layout. • Section numbers removed. • Updated drawing in section 1.2 to show buffer columns and rows. • Updated section 1.4.1 Monochrome Quantum Efficiency. • Updated section 1.4.3 CFA pattern to show buffer columns and rows. • Updated section 1.9 Quality Assurance and Reliability. • Added section 1.10.1 Available Part Configurations. • Updated section 3.1 Pin Grid Array Package Cover Glass. Glass changed from clear to MAR. Updated section 3.3 Glass Transmission. • Section 4.11.2 Bias Voltages, changed V1MID and V2 MID from • min –1.5, nom –1.0, max –0.5 to • min –1.5, nom –1.2, max –1.0 • Section 4.11.2 Added power up sequence note.
4.0	• Corrected figure on page 4. Buffers rows and columns were incorrect. Changed from 4 rows/columns to 2 rows/columns. • Corrected figure on page 8. Buffers rows and columns were incorrect. Changed from 4 rows/columns to 2 rows/columns.
4.1	• Added to the CDS Output Specification table an Output Bias Current nominal value. • Correlated Double Sampling (CDS) Section – Last sentence changed from "The A and B outputs of the CDS circuit will be in the range of 7 to 9 volts." to "The A and B outputs of the CDS circuit will be in the range of 7 to 11 volts.". This matches the change made in revision 2.0. • Updated schematic to show two diodes for V1MID and V2MID power supply. Corrected sentences below schematics from "The V1MID and V2MID connections must be set to –0.6 to –1.5V. Since V1MID and V2MID only sink current, one diode can be used to set this voltage." to "The V1MID and V2MID connections must be set to –1.0 to –1.5V. Since V1MID and V2MID only sink current, two diodes can be used to set this voltage. This change is to match the update in revision 3.0. • Updated schematic – addition of D4, which sets the V1MID and V2MID voltage to –1.2V.
5.0	• Updated format • Updated pictures on Summary Specification page • Added sampling plan to performance parameters • Update evaluation board pictures • Merged MTD-PS-0293 KAI-1020 Test Supplement specification into this document
6.0	• Added the note "Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions*" to the following sections • Operation, Electronic Shutter • Camera Design, Electronic Shutter • Storage and Handling • Changed cover glass material to D263T eco or equivalent

PS-0019

Revision Number	Description of Changes
1.0	• Initial release with new document number, updated branding and document template • Updated *Storage and Handling* and *Quality Assurance and Reliability* sections • Reorganized structure for consistency with other Interline Transfer CCD documents
2.0	• Added Monochrome, Telecentric Microlens, PGA Package, Taped Clear Cover Glass (no coatings) part numbers to the Ordering Information table
2.1	• Updated branding

PUBLICATION ORDERING INFORMATION

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