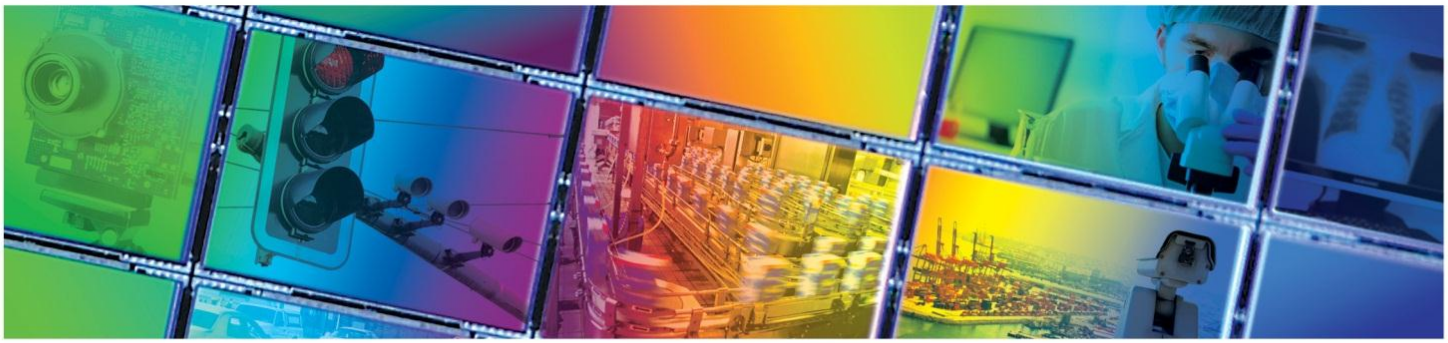
ON Semiconductor®

KAC-12040 IMAGE SENSOR

4000 (H) X 3000 (V) CMOS IMAGE SENSOR



JUNE 13, 2014

DEVICE PERFORMANCE SPECIFICATION

REVISION 1.3 PS-0143

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KAC-12040 Image Sensor

DESCRIPTION

The KAC-12040 Image Sensor is a high-speed 12 megapixel CMOS image sensor in a 4/3" optical format based on a 4.7 µm 5T CMOS platform. The image sensor features very fast frame rate, excellent NIR sensitivity, and flexible readout modes with multiple regions of interest (ROI). The readout architecture enables use of 8, 4, or 2 LVDS output banks for full resolution readout of 70 frames per second.

Each LVDS output bank consists of up to 8 differential pairs operating at 160 MHz DDR for a 320 Mbps data rate per pair. The pixel architecture allows rolling shutter operation for motion capture with optimized dynamic range or global shutter for precise still image capture.

The image sensor has a pre-configured QFHD (4 x 1080p, 16:9) video mode, fully programmable, multiple ROI for windowing, programmable sub-sampling, and reverse readout (flip and mirror). The two ADCs can be configured for 8-bit, 10-bit, 12-bit or 14-bit conversion and output.

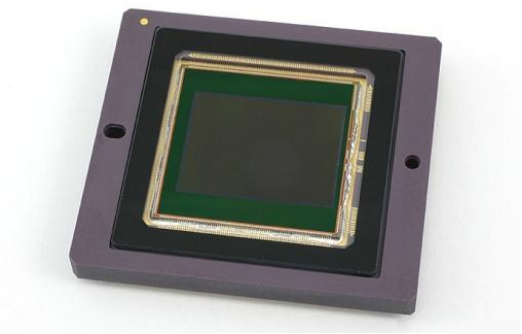
Additional features include interspersed video streams (dual-video), on-chip responsivity calibration, black clamping, overflow pixel for blooming reduction, black-sun correction (anti-eclipse), column and row noise correction, and integrated timing generation with SPI control, 4:1 and 9:1 averaging decimation modes.

FEATURES

- Global shutter and rolling shutter
- Very fast frame rate
- High NIR sensitivity
- Multiple regions of interest
- Interspersed video streams

APPLICATIONS

- Machine Vision
- Intelligent Transportation Systems
- Surveillance



Parameter	Typical Value
Architecture	5T Global Shutter CMOS
Resolution	12 megapixels
Aspect Ratio	4:3
Pixel Size	4.7 µm (H) x 4.7 µm (V)
Total Number of Pixels	4224 (H) x 3192 (V)
Number of Effective Pixels	4016 (H) x 3016 (V)
Number of Active Pixels	4000 (H) x 3000 (V)
Active Image Size	18.8 mm (H) x 14.1 mm (V) 23.5 mm (diag.), 4/3" optical format
Master Clock Input Speed	5 MHz to 50 MHz
Maximum Pixel Clock Speed	160 MHz DDR LVDS, 320 Mbps
Number of LVDS Outputs	64 differential pairs
Number of Output Banks	8, 4, or 2
Frame Rate, 12 MP	1 - 70 fps 10 bits 1 - 75 fps 8 bits
Charge Capacity	16,000 electrons
Quantum Efficiency KAC-12040-CBA KAC-12040-ABA	 40%, 47%, 45% (470, 540, 620 nm) 53%, 15%, 10% (500, 850, 900 nm)
Read Noise (at maximum LVDS clock)	3.7 e^- rms, Rolling Shutter 25.5 e^- rms, Global Shutter
Dynamic Range	73 dB, Rolling Shutter 56 dB, Global Shutter
Blooming Suppression	>10,000x
Image Lag	1.3 electron
Digital Core Supply	2.0 V
Analog Core Supply	1.8 V
Pixel Supply	2.8 V & 3.5 V
Power Consumption	1.5 W for 12 Mp @ 70 fps 10 bits
Package	267 pin ceramic micro-PGA
Cover Glass	AR Coated, 2-sides

All parameters are specified at T = 40 °C unless otherwise noted

Ordering Information

KAC-12040 Image Sensor

Catalog Number	Product Name	Description	Marking Code
4H2227	KAC-12040-ABA-JD-AA	Monochrome, micro-PGA Package, Sealed Clear Cover Glass with AR coating(both sides), Standard Grade	KAC-12040-ABA Serial Number
4H2229 (1)	KAC-12040-ABA-JD-AE	Monochrome, micro-PGA Package, Sealed Clear Cover Glass with AR coating(both sides), Engineering Grade	
4H2231	KAC-12040-CBA-JD-AA	Bayer (RGB) Color Filter Pattern, micro-PGA Package, Sealed Clear Cover Glass with AR coating(both sides), Standard Grade	KAC-12040-CBA Serial Number
4H2233 (1)	KAC-12040-CBA-JD-AE	Bayer (RGB) Color Filter Pattern, micro-PGA Package, Sealed Clear Cover Glass with AR coating(both sides), Engineering Grade	

Notes:
1. Engineering Grade samples might not meet final production testing limits, especially for cosmetic defects such as clusters, but also possibly column and row artifacts. Overall performance is representative of final production parts.

Evaluation Support

Catalog Number	Product Name	Description
4H2290	KEK-4H2290-KAC-12040-CB	Evaluation Hardware for KAC-12040 Image Sensor (color). Includes Image Sensor.
4H2291	KEK-4H2291-KAC-12040-AB	Evaluation Hardware for KAC-12040 Image Sensor (monochrome). Includes Image Sensor.
4H2211	Lens Mount Kit	Lens Mount Kit that supports C, CS, and F mount lenses. Includes IR cut-filter for color imaging.

See Application Note Product Naming Convention for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.truesenseimaging.com.

Please address all inquiries and purchase orders to:

Truesense Imaging, Inc.
1964 Lake Avenue
Rochester, New York 14615

Phone: (585) 784-5500
E-mail: info@truesenseimaging.com

Device Description

ARCHITECTURE

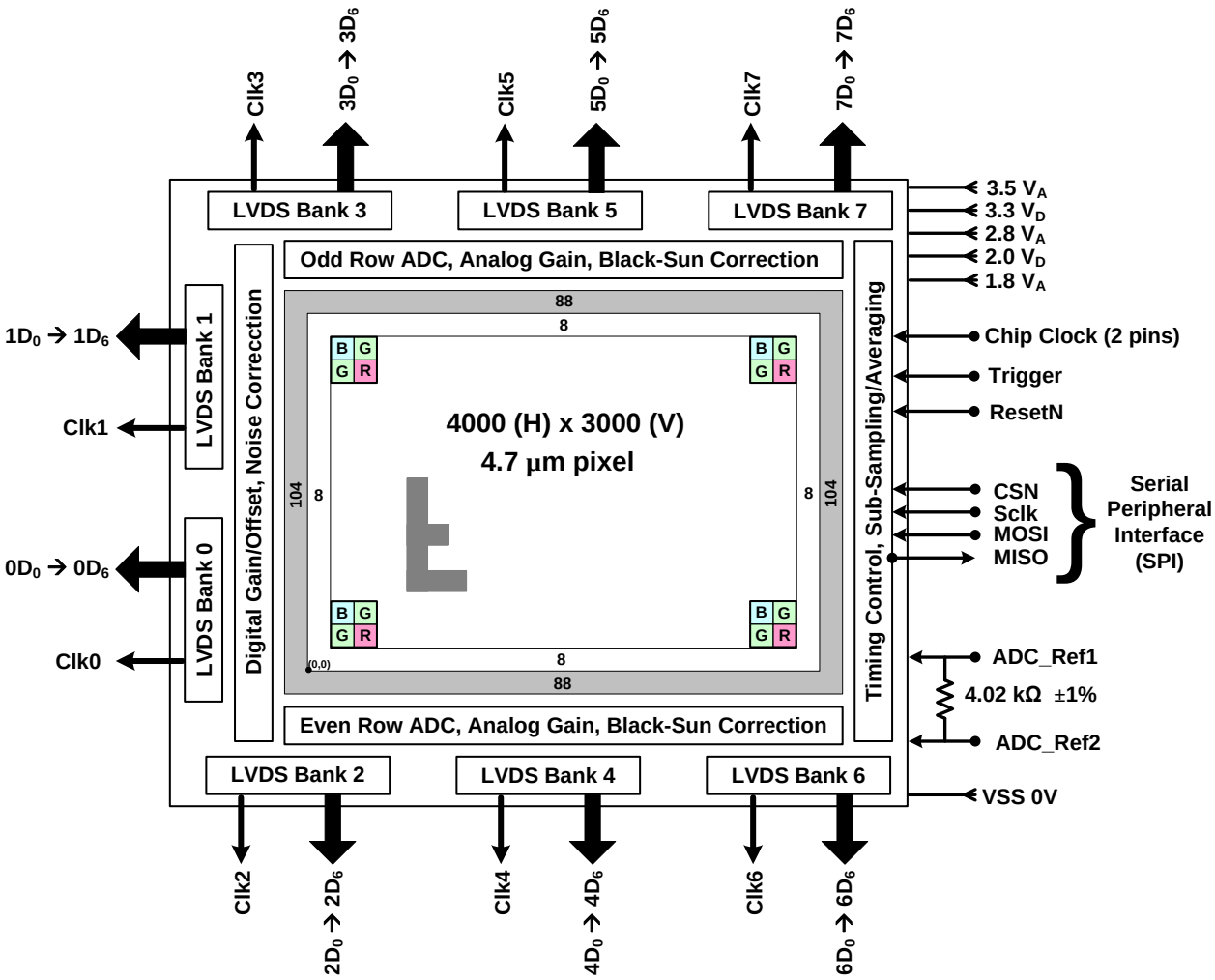


Figure 1: Block Diagram

PHYSICAL ORIENTATION

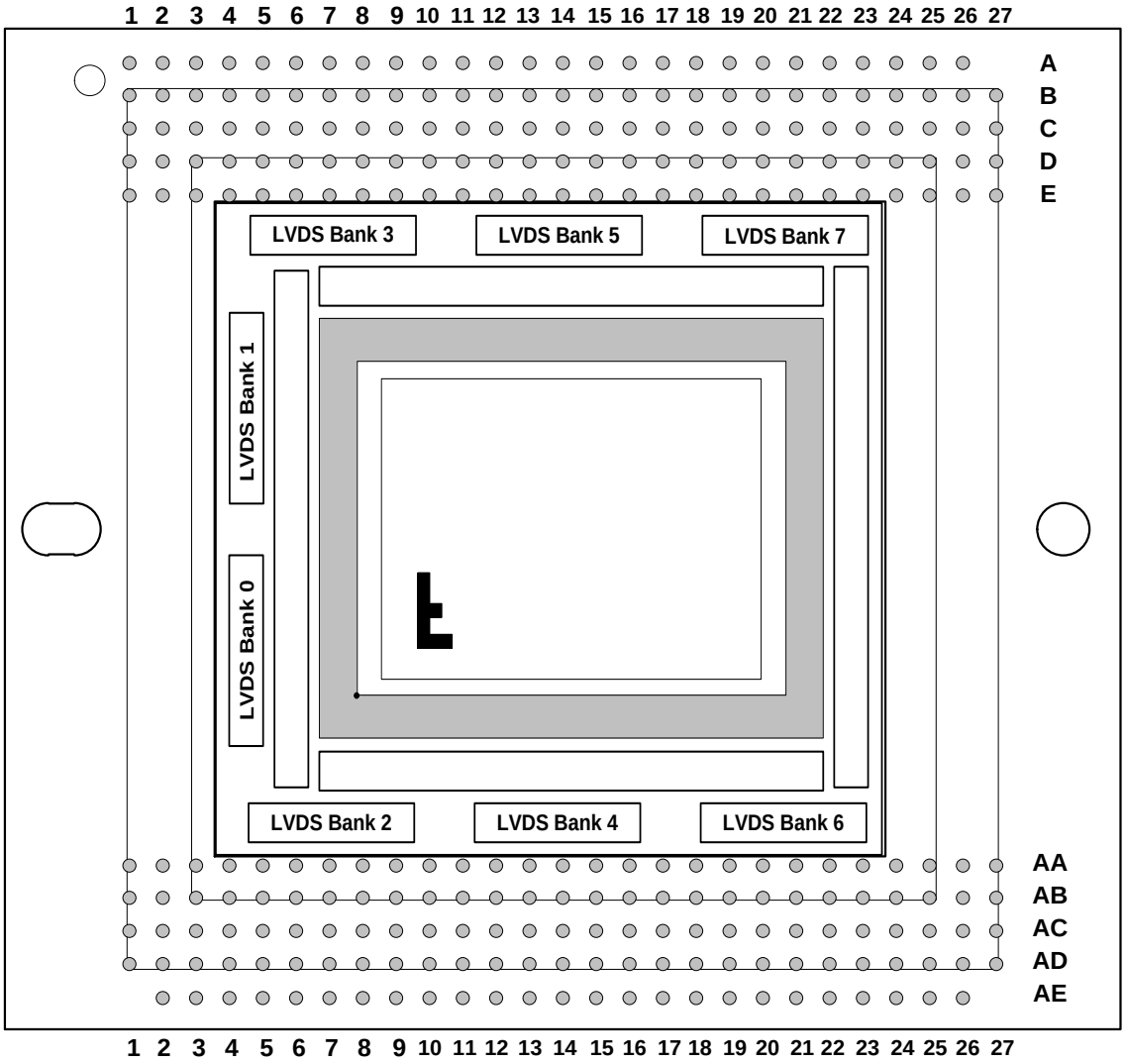


Figure 2: Package Pin Orientation – Top x-ray view

Notes:

1. The center of the pixel array is aligned to the physical package center.
2. The region under the sensor die is clear of pins enabling the use of a heat sink.
3. Non-symmetric mounting holes provide orientation and mounting precision.
4. Non-symmetric pins prevent incorrect placement in PCB.
5. Letter “F” indicator shows default readout direction relative to package pin 1

PRIMARY PIN DESCRIPTION

Pin	Name	Type	Description
AB09	RESETN	DI	Sensor reset (0 V = Reset State)
E07	CLK_In1	DI	Sensor Input Clk_In1 (45 – 50 MHz)
D08	CLK_In2	DI	Sensor Input Clk_In2 (connect to Clk1)
AB08	TRIGGER	DI	Trigger input (optional)
AA05	SCLK	DI	SPI Master Clock
AA08	MOSI	DI	SPI Master Output Slave Input
AA07	MISO	DO	SPI Master Input, Slave Output
AA06	CSN	DI	SPI Chip Select (0 V = Selected)
AA14	ADC_Ref1	AO	4.02 kΩ ±1% resistor between Ref1 & Ref2
AA15	ADC_Ref2	AO	4.02 kΩ ±1% resistor between Ref1 & Ref2
AB07	MSO	DO	Mechanical Shutter output sync (optional)
AB06	FLO	DO	Flash output sync (optional)
E05	FEN	DO	Frame ENable reference output (optional)
E06	LEN	DO	Line ENable reference output (optional)

Notes:

1. DI = Digital Input, DO = Digital Output, AO = Analog Output
2. Tie unused DI pins to Ground, NC unused DO pins
3. By default Clk_In2 should equal Clk_In1 and should be the same source clock.
4. The RESETN pin has a 62 kΩ internal pull-up resistor, so if left floating the chip will not be in reset mode.
5. The TRIGGER pin has an internal 100 kΩ pull down resistor. If left floating (and at default polarity) then the sensor state will not be affected by this pin (ie defaults to 'not triggered' mode if floated)
6. All of the DI and DO pins nominally operate at 0 V → 2.0 V and are associated with the VDD_DIG power supply.

POWER PIN DESCRIPTION

Name	Voltage	Pins	Description
VDD_LVDS	3.3V D	C04, C05, C23, C24, D04, D24, E04, E24, AA04, AA24, AB04, AB24, AC04, AC05, AC23, AC24	LVDS output supply
VDD_DIG	2.0V D	C18, C19, D18, D19, E18, AA18, AB18, AB19, AC18, AC19, C20, C21, C22, D20, D21, D22, D23, E20, E21, E22, AA20, AA21, AA22, AB20, AB21, AB22, AB23, AC20, AC21, AC22, AB15, E08	Digital core supply
AVDD_HV	3.5V A	C11, D11, E11, AA11, AB11, AC11, C10, D10, E10, AA10, AB10, AC10	Pixel supply 1
Vref_P	2.8V A	C13, D13, E13, AA13, AB13, AC13	Pixel supply 2
AVDD_LV	1.8V A	C17, D16, D17, E17, AA17, AB16, AB17, AC17	Analog low voltage supply
Vpixel_low	0 V	E09	Pixel Supply 3. Combine with VSS for normal operation. Can be pulsed for Extended Dynamic Range Operation
VSS	0 V	C12, C14, D12, D14, E12, AA12, AB12, AB14, AC12, AC14, E15, D15, AA09, A02, A14, A26, B14, C03, C06, C25, D03, D25, E03, E19, E23, E25, AA03, AA19, AA23, AA25, AB03, AB25, AC03, AC06, AC25, AD14, AE02, AE14, AE26	Sensor ground reference
No Connect	NA	A01, AC09, E14, E16, C09, D09, D05, D06, D07, AA16, AB05	Unused and test-only pins. These pins must be floated.

LVDS Pin Description

Pin	Name	Descr
E01	1DCLK+	Bank 1 LVDS Clock
E02	1DCLK-	
D01	1DATA0+	Bank 1 LVDS Data
D02	1DATA0-	
C01	1DATA1+	
C02	1DATA1-	
B01	1DATA2+	
B02	1DATA2-	
A03	1DATA3+	
B03	1DATA3-	
A04	1DATA4+	
B04	1DATA4-	
A05	1DATA5+	
B05	1DATA5-	
A06	1DATA6+	
B06	1DATA6-	

Pin	Name	Descr
C07	3DCLK+	Bank 3 LVDS Clock
C08	3DCLK-	
A07	3DATA0+	Bank 3 LVDS Data
B07	3DATA0-	
A08	3DATA1+	
B08	3DATA1-	
A09	3DATA2+	
B09	3DATA2-	
A10	3DATA3+	
B10	3DATA3-	
A11	3DATA4+	
B11	3DATA4-	
A12	3DATA5+	
B12	3DATA5-	
A13	3DATA6+	
B13	3DATA6-	

Pin	Name	Descr
C15	5DCLK+	Bank 5 LVDS Clock
C16	5DCLK-	
A15	5DATA0+	Bank 5 LVDS Data
B15	5DATA0-	
A16	5DATA1+	
B16	5DATA1-	
A17	5DATA2+	
B17	5DATA2-	
A18	5DATA3+	
B18	5DATA3-	
A19	5DATA4+	
B19	5DATA4-	
A20	5DATA5+	
B20	5DATA5-	
A21	5DATA6+	
B21	5DATA6-	

Pin	Name	Descr
A22	7DCLK+	Bank 7 LVDS Clock
B22	7DCLK-	
A23	7DATA0+	Bank 7 LVDS Data
B23	7DATA0-	
A24	7DATA1+	
B24	7DATA1-	
A25	7DATA2+	
B25	7DATA2-	
B27	7DATA3+	
B26	7DATA3-	
C27	7DATA4+	
C26	7DATA4-	
D27	7DATA5+	
D26	7DATA5-	
E27	7DATA6+	
E26	7DATA6-	

Pin	Name	Descr
AA01	0DCLK+	Bank 0 LVDS Clock
AA02	0DCLK-	
AB01	0DATA0+	Bank 0 LVDS Data
AB02	0DATA0-	
AC01	0DATA1+	
AC02	0DATA1-	
AD01	0DATA2+	
AD02	0DATA2-	
AE03	0DATA3+	
AD03	0DATA3-	
AE04	0DATA4+	
AD04	0DATA4-	
AE05	0DATA5+	
AD05	0DATA5-	
AE06	0DATA6+	
AD06	0DATA6-	

Pin	Name	Descr
AC07	2DCLK+	Bank 2 LVDS Clock
AC08	2DCLK-	
AE07	2DATA0+	Bank 2 LVDS Data
AD07	2DATA0-	
AE08	2DATA1+	
AD08	2DATA1-	
AE09	2DATA2+	
AD09	2DATA2-	
AE10	2DATA3+	
AD10	2DATA3-	
AE11	2DATA4+	
AD11	2DATA4-	
AE12	2DATA5+	
AD12	2DATA5-	
AE13	2DATA6+	
AD13	2DATA6-	

Pin	Name	Descr
AC15	4DCLK+	Bank 4 LVDS Clock
AC16	4DCLK-	
AE15	4DATA0+	Bank 4 LVDS Data
AD15	4DATA0-	
AE16	4DATA1+	
AD16	4DATA1-	
AE17	4DATA2+	
AD17	4DATA2-	
AE18	4DATA3+	
AD18	4DATA3-	
AE19	4DATA4+	
AD19	4DATA4-	
AE20	4DATA5+	
AD20	4DATA5-	
AE21	4DATA6+	
AD21	4DATA6-	

Pin	Name	Descr
AE22	6DCLK+	Bank 6 LVDS Clock
AD22	6DCLK-	
AE23	6DATA0+	Bank 6 LVDS Data
AD23	6DATA0-	
AE24	6DATA1+	
AD24	6DATA1-	
AE25	6DATA2+	
AD25	6DATA2-	
AD26	6DATA3+	
AD27	6DATA3-	
AC26	6DATA4+	
AC27	6DATA4-	
AB26	6DATA5+	
AB27	6DATA5-	
AA26	6DATA6+	
AA27	6DATA6-	

Notes:

1. All LVDS Data and Clock lines must be routed with 100 Ω differential transmission line traces.
2. All the traces for a single LVDS Bank should be the same physical length to minimize skew between the clock and data lines.
3. In 2 Bank mode, only LVDS banks 0 and 1 are active.
4. In 4 Bank mode, only LVDS bank 0, 1, 2, and 3 are active.
5. Float the pins of unused LVDS Banks to conserve power.
6. Unused pins in active banks (due to ADC bit depth <14) are automatically tri-stated to save power, but these can also be floated.

Imaging Performance

Typical Operation Conditions

Unless otherwise noted, the Imaging Performance Specifications are measured using the following conditions.

Description	Condition	Notes
Light Source	Continuous red, green and blue LED illumination	1
Temperature	Measured die temperature: 40 °C and 27 °C	
Integration Time	16.6 msec (1400d LL, register 0201h)	
Readout Mode	Dual-Scan, Global Shutter, 320 MHz PLL2	
Clamps	Column/Row Noise Correction active, Frame Black Level Clamp active	
ADC Bit Depth	10 bit	
Analog Gain	Unity gain or referred back to unity gain.	

Notes:

1. For monochrome sensor, only green LED used.

Performance Specifications All Configurations

Description	Symbol	Min.	Nom.	Max.	Units	Sampling Plan	Temperature Tested At (°C)	Test	Notes
Photodiode Charge Capacity	PNe	-	16	-	ke$^-$	Die	27, 40	16	
Read Noise	ne-T	-	3.7 RS 25.5 GS	-	e$^-$rms	Die	27	8	
Total Pixelized Noise		-	4.5 RS 28.3 GS	-	e$^-$rms	Die	27	19	
Dynamic Range	DR	-	73 RS 56 GS	-	dB	Die	27		3
Column Noise	Cn	-	0.6 RS 3.0 GS	-	e$^-$rms	Die	27	9	5
Row Noise	Rn	-	1.0 RS 5.0 GS	-	e$^-$rms	Die	27	10	6
Dark Field Local Non-Uniformity Floor	DSNU_flr	-	3.0 RS 21 GS	-	e$^-$rms	Die	27 & 40	1	4
Bright Field Global Photoresponse Non-Uniformity	PRNU_1	-	1.5	-	%rms	Die	27, 40	2	1
Bright Field Global Peak to Peak Photoresponse Non-Uniformity	PRNU_2	-	6.5	-	%pp	Die	27, 40	3	1
Maximum Photoresponse Nonlinearity	NL	-	6.3	-	%	Die	27, 40	11	2
Maximum Gain Difference Between Outputs	ΔG	-	0.3	-	%	Die	27, 40	12	7
Photodiode Dark Current	Ipd	-	4.6	70	e/p/s	Die	40	13	8
Storage Node Dark Current	Ivd	-	1200	5000	e/p/s	Die	40	14	4
Image Lag	Lag	-	1.3	10	e$^-$	Design	27, 40	15	
Black-Sun Anti-Blooming	Xab	-	12 >10,000	-	W/cm^2 xIllumSat	Design	27	7	13
Parasitic Light Sensitivity	PLS	-	730	-	-	Design	27	6	9
Dual-Video WDR		-	140 RS 120 GS	-	dB	Design	27		10, 11
Pulsed Pixel WDR (GS only)		-	100	-	dB	Design	27		12, 11

RS = Rolling Shutter operation mode, GS = Global Shutter operation mode

KAC-12040-ABA Configuration (Monochrome)

Description		Symbol	Wavelength (nm)	Min.	Nom.	Max	Units	Sampling Plan	Temperature Tested At (°C)	Test
Peak Quantum Efficiency	Green NIR1 NIR2	QE_{max}	550 850 900	-	53 15 10	-	%	Design	27	
Responsivity				-	84	-	$\frac{ke^-}{Lux * s}$	Design	27	20
Responsivity				-	7.0	-	$\frac{V}{Lux * s}$	Design	27	21

KAC-12040-CBA Configuration (Bayer RGB)

Description		Symbol	Wavelength (nm)	Min.	Nom.	Max	Units	Sampling Plan	Temperature Tested At (°C)	Test
Peak Quantum Efficiency	Green NIR1 NIR2	QE_{max}	470 540 620 850 900	-	40 47 45 15 10	-	%	Design	27	
Responsivity			Blue Green Red	-	17 35 38	-	$\frac{ke^-}{Lux * s}$	Design	27	20
Responsivity			Blue Green Red	-	1.4 2.9 3.2	-	$\frac{V}{Lux * s}$	Design	27	21

Notes:

1. Measured per color, worst of all colors reported
2. Value is over the range of 10% to 90% of photodiode saturation, Green response used.
3. Uses 20LOG(PNe/ ne-T)
4. Photodiode dark current made negligible
5. Column Noise Correction active
6. Row Noise Correction active
7. Measured at ~70% illumination
8. Storage node dark current made negligible
9. GSE (Global Shutter Efficiency) = 1-1/PLS
10. Min vs Max integration time at 30 fps
11. WDR measures expanded exposure latitude from linear mode DR
12. Min/Max responsivity in a 30 fps image
13. Saturation Illumination referenced to a 3 line time integration.

Typical Performance Curves

QUANTUM EFFICIENCY

Monochrome with Microlens

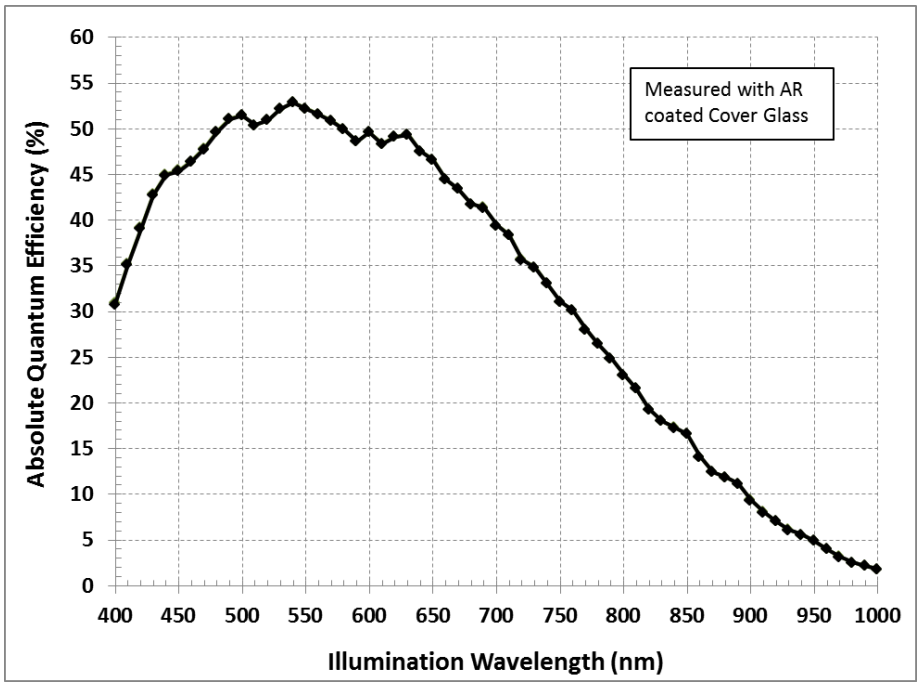


Figure 3: Monochrome QE (with Microlens)

Color (Bayer RGB) with Microlens

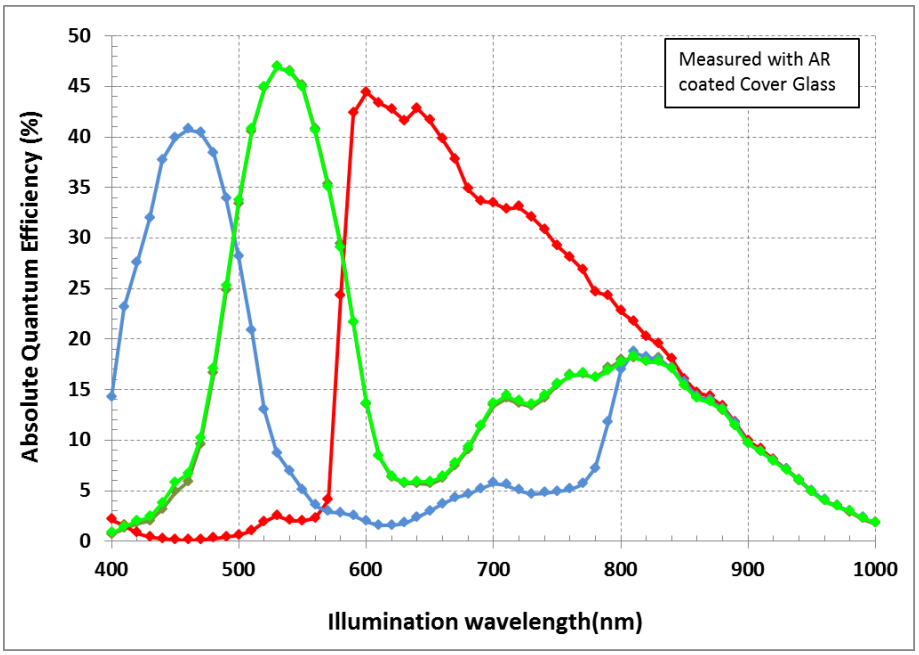


Figure 4: Bayer QE (with Microlens)

ANGULAR QUANTUM EFFICIENCY

For the curves marked “Horizontal”, the incident light angle is varied along the wider array dimension.

For the curves marked “Vertical”, the incident light angle is varied along the shorter array dimension.

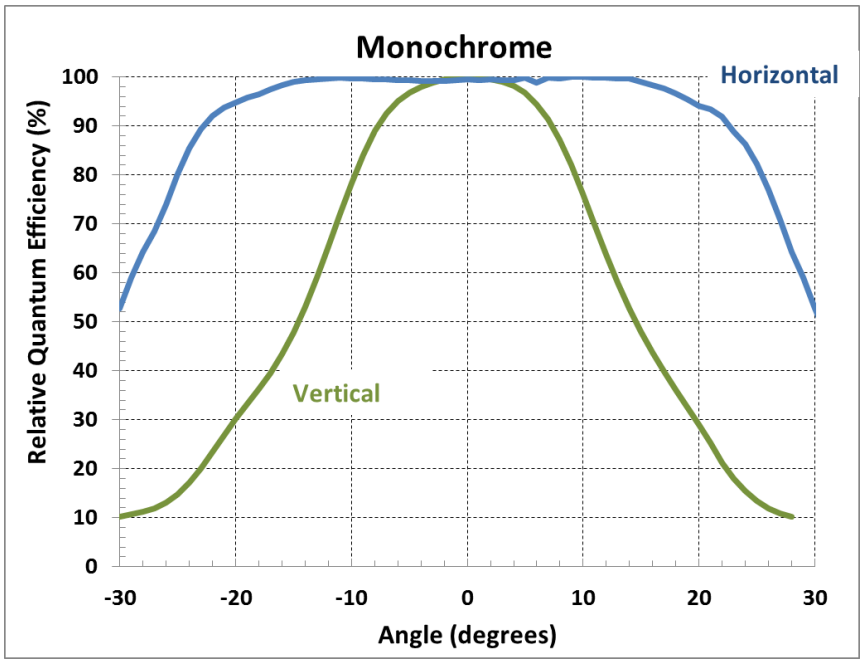


Figure 5: Monochrome Relative Angular QE (with Microlens)

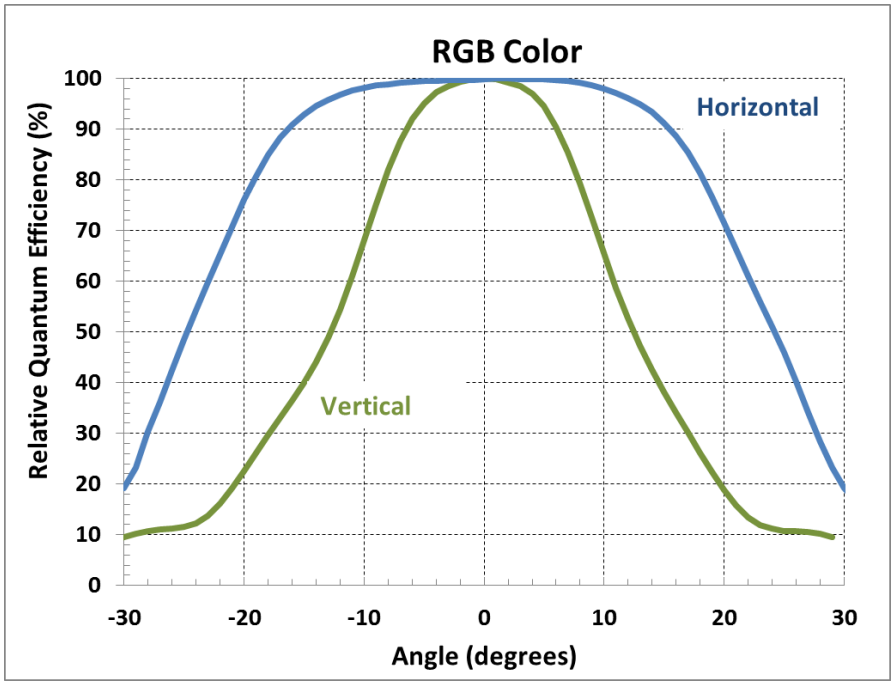


Figure 6: Bayer Relative Angular QE (with Microlens)

DARK CURRENT VERSUS TEMPERATURE

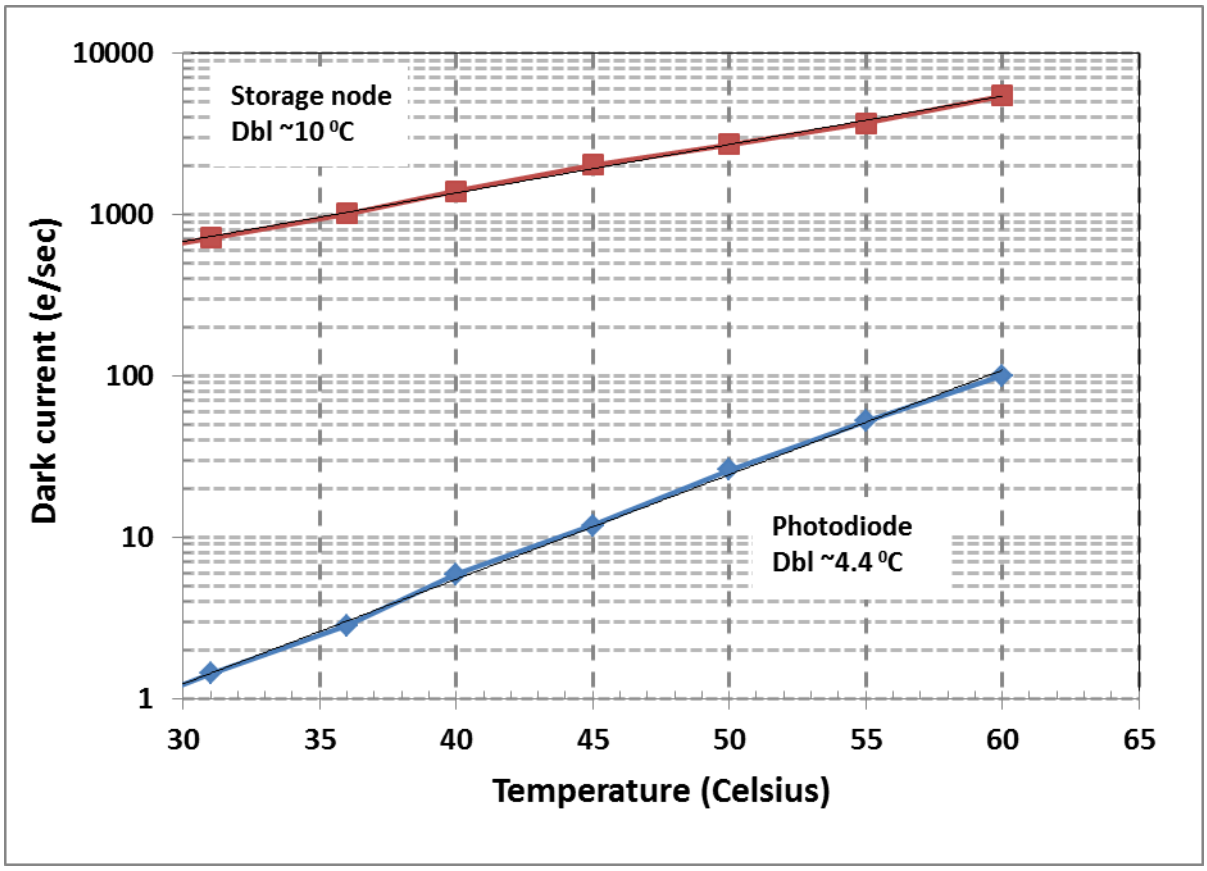


Figure 7: Dark Current vs Temperature

Note: "Dbl" denotes an approximate doubling temperature for the dark current for the displayed temperature range.

POWER VS FRAME RATE

The most effective method to use the maximum PLL2 speed (313 -> 320 MHz) and control frame rate with minimum Power and maximum image quality is to adjust Vertical Blanking. (register 01F1h). Unnecessary chip operations are suspended during Vertical Blanking conserving significant power consumption and also minimizing the image storage time on the storage node when in Global Shutter Operation.

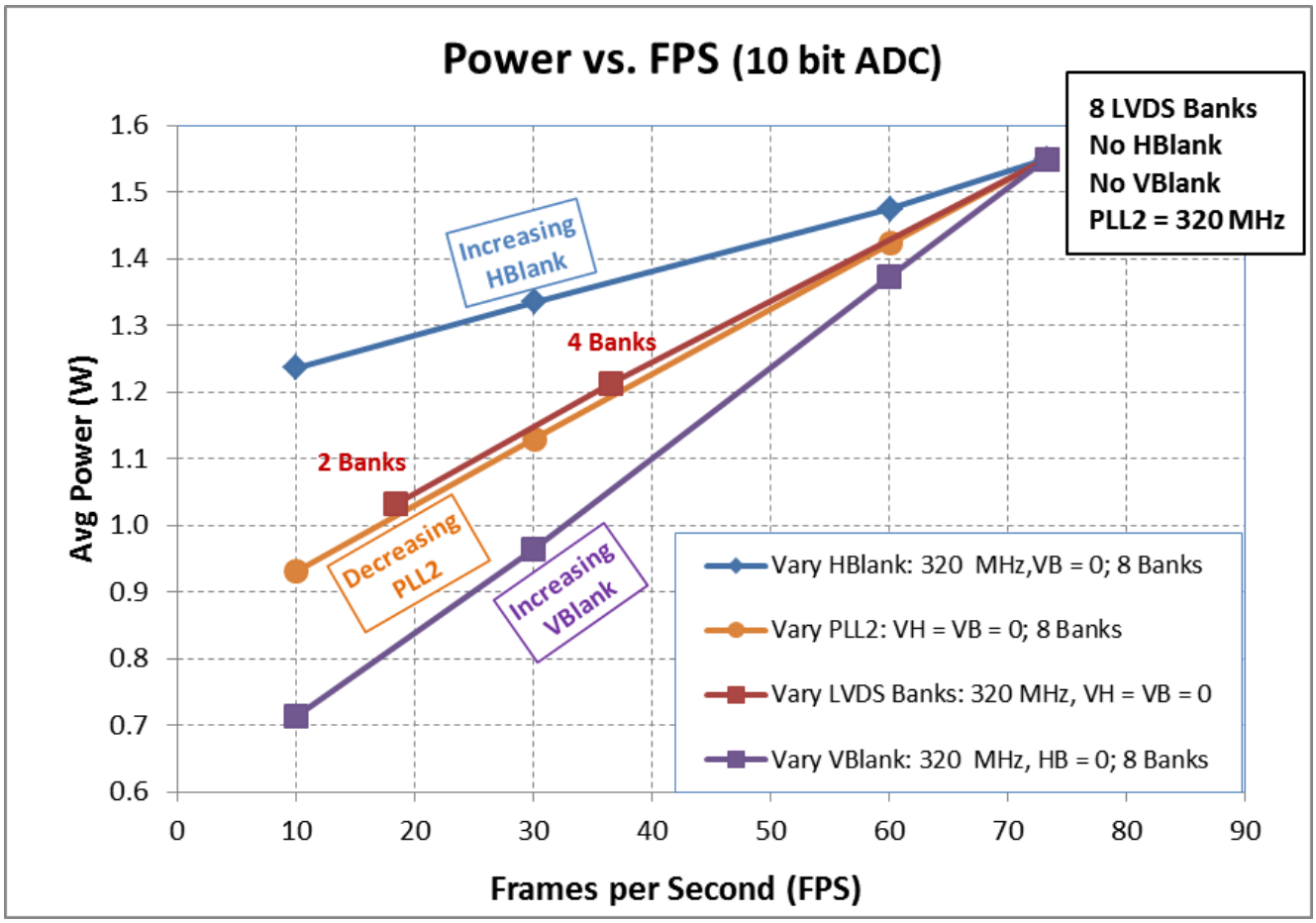


Figure 8: Power vs Frame Rate, 10 bit mode

Notes:

1. The LVDS clock is ½ the PLL2 clock speed

Power and Frame Rate vs ADC Bit depth

Increasing the ADC bit depth impacts the frame rate by changing the ADC conversion time. The following figure shows the power and Frame rate range for several typical cases.

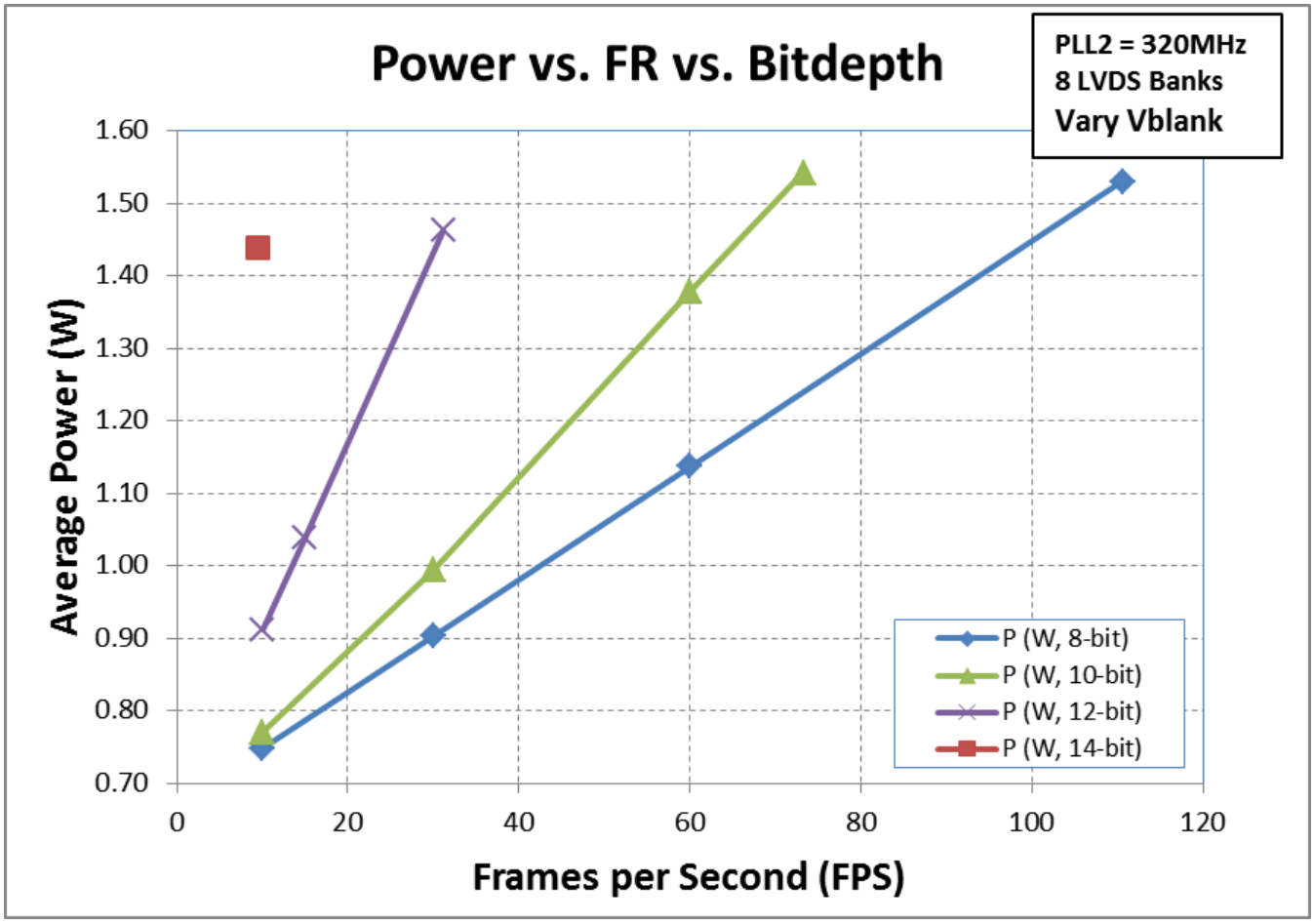


Figure 9: ADC Bit Depth impact on Frame Rate and Power

Defect Definitions

Operation Conditions for Defect Testing

Description	Condition	Notes
Operational Mode	10 bit ADC, 8 LVDS outputs, Global Shutter and Rolling Shutter modes, Dual-Scan, Black Level Clamp on, Column/Row Noise Correction on, 1x Analog Gain, 1x Digital Gain	
Pixels Per Line	4000	
Lines Per Frame	3000	
Line Time	8.7 µsec	
Frame Time	13.9 msec	
Photodiode Integration Time	33 msec	
Storage Readout Time	13.9 msec	
Temperature	40 °C and 29 °C	
Light Source	Continuous red, green and blue LED illumination	1
Operation	Nominal operating voltages and timing, PLL1 = 320 MHz, PLL2 = 320 MHz, Wafer Test	

Notes:
1. For monochrome sensor, only the green LED is used.

Defect Definitions for Testing

Description	Definition		Limit	Test	Notes
Dark Field Defective Pixel	30 °C RS: Defect ≥ 20 dn GS: Defect ≥ 180 dn	40 °C RS: Defect ≥ 30 dn GS: Defect ≥ 240 dn	120	4	3, 4
Bright Field Defective Pixel	Defect ≥ ±12% from local mean			5	1, 4
Cluster Defect	A group of 2 to 10 contiguous defective pixels, but no more than 3 adjacent defects horizontally		22		2
Column/Row Major Defect	A group of more than 10 contiguous defective pixels along a single column or row		0		
Dark Field Faint Column/Row Defect	RS: 3 dn threshold GS: 10 dn threshold		0	17	
Bright Field Faint Column/Row Defect	RS: 12 dn threshold GS: 18 dn threshold		0	18	

Notes:
RS = Rolling Shutter, GS = Global Shutter
1. For the color devices, all bright defects are defined within a single color plane, each color plane is tested
2. Cluster defects are separated by no less than two good pixels in any direction.
3. Rolling Shutter Dark Field points are dominated by photodiode integration time, Global Shutter Dark Field defects are dominated by the readout time.
4. The net sum of all bright and dark field pixel defects in rolling and global shutter are combined and then compared to the test limit

Defect Map

The defect map supplied with each sensor is based upon testing at an ambient (29 °C) temperature. All defective pixels are reference to pixel (0, 0) in the defect maps. See Figure 10 for the location of pixel (0, 0).

Test Definitions

TEST REGIONS OF INTEREST

Image Area ROI: Pixel (0, 0) to Pixel (4015, 3015)

Active Area ROI: Pixel (8, 8) to Pixel (3999, 2999)

Center ROI: Pixel (1958, 1458) to Pixel (2057, 1557)

Only the Active Area ROI pixels are used for performance and defect tests.

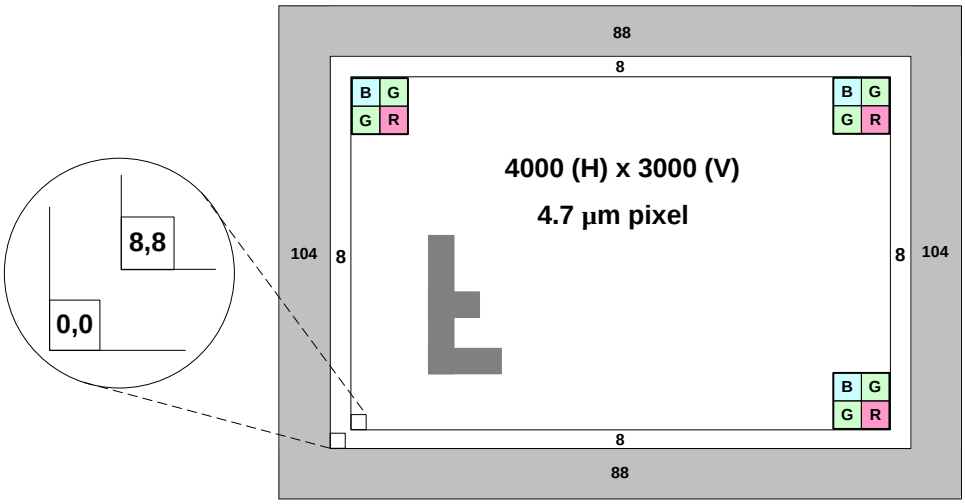


Figure 10: Regions of Interest

TEST DESCRIPTIONS

1) Dark Field Local Non-Uniformity Floor (DSNU_flr)

This test is performed under dark field conditions. A 4 frame average image is collected. This image is partitioned into 300 sub-regions of interest, each of which is 200 by 200 pixels in size. For each sub-region the standard deviation of all its pixels is calculated. The dark field local non-uniformity is the largest standard deviation found from all the sub regions of interest. Units: e^- rms (electrons rms)

2) Bright Field Global Photoresponse Non-Uniformity (PRNU_1)

The sensor illuminated to 70% of saturation (~700 dn). In this condition a 4 frame average image is collected. From this 4 frame average image a 4 frame average dark image is subtracted. The Active Area Standard Deviation is the standard deviation of the resultant image and the Active Area Signal is the average of the resultant image.

$$PRNU\_1 = 100 * \left(\frac{\text{Active Area Standard Deviation}}{\text{Active Area Signal}} \right)$$ Units: %rms

3) Bright Field Global Peak to Peak Non-Uniformity (PRNU_2)

This test is performed with the sensor uniformly illuminated to 70% of saturation (~700 dn), a 4 frame average image is collected and a 4 frame averaged dark image is subtracted. The resultant image is partitioned into 300 sub regions of interest, each of which is 200 by 200 pixels in size. The average signal level of each sub regions of interest (sub-ROI) is calculated.

The highest sub-ROI average (Maximum Signal) and the lowest sub-ROI average (Minimum Signal) are then used in the following formula to calculate PRNU_2.

$$PRNU\_2 = 100 * \frac{Maximum\ Signal\ -\ Minimum\ Signal}{Active\ Area\ Signal}$$ Units: %pp

4) Dark Field Defect Test

This test is performed under dark field conditions. The sensor is partitioned into 300 sub regions of interest, each of which is 128 by 128 pixels in size. In each region of interest, the median value of all pixels is found. For each region of interest, a pixel is marked defective if it is greater than or equal to the median value of that region of interest plus the defect threshold specified in the Defect Definition Table section.

5) Bright Field Defect Test

This test is performed with the imager illuminated to a level such that the output is at approximately 700 dn. The average signal level of all active pixels is found. The bright and dark thresholds are set as:

Dark defect threshold = Active Area Signal * threshold

Bright defect threshold = Active Area Signal * threshold

The sensor is then partitioned into 300 sub regions of interest, each of which is 128 by 128 pixels in size. In each region of interest, the average value of all pixels is found. For each region of interest, a pixel is marked defective if it is greater than or equal to the median value of that region of interest plus the bright threshold specified or if it is less than or equal to the median value of that region of interest minus the dark threshold specified.

Example for bright field defective pixels:

- Average value of all active pixels is found to be 700 dn
- Lower defect threshold: 700 dn * 12 % = 84 dn
- A specific 128 x 128 ROI is selected:
    - Median of this region of interest is found to be 690 dn.
    - Any pixel in this region of interest that is ≤ (690 - 84 dn) in intensity will be marked defective.
    - Any pixel in this region of interest that is ≥ (690 - 84 dn) in intensity will be marked defective
- All remaining 299 sub regions of interest are analyzed for defective pixels in the same manner.

6) Parasitic Light Sensitivity (PLS)

Parasitic Light Sensitivity is the ratio of the light sensitivity of the photodiode to the light sensitivity of the storage node in Global Shutter. There is no equivalent distortion in Rolling Shutter. A low PLS value can provide distortion of the image on the storage node by the scene during readout.

$$PLS = \frac{Photodiode\ Responsivity}{Storage\ Node\ Responsivity} \qquad \text{(unitless ratio)}$$

GSE (Global Shutter Efficiency) is a related unit. $GSE = \left(1 - \frac{1}{PLS}\right)\ \%$

Detailed method: Photodiode Responsivity:

> The sensor is set in global shutter serial mode (integration time not overlapping readout) and the FLO signal is used to control a 550 nm normal incident (or large f# focused) illumination source so that the sensor is illuminated only during photodiode integration time (not illuminated during readout time). The integration time is not critical but should be large enough to create a measurable mean during this time. A 16 frame-average illuminated photodiode image is recorded. A 16 frame-average dark frame using the same sensor settings is captured and is subtracted from the illuminated image.

Detailed method: Storage Node Responsivity:

> The sensor is set to a special characterization mode where the PD signal is discarded and does not impact the storage node. A long total frame time (storage node exposure time) is used to increase the storage node signal. A 16 frame-average dark frame is captured. The sensor is illuminated by the same 550nm incident light source used for the photodiode responsivity. A 16 frame-average illuminated photodiode image is recorded; the dark frame image is subtracted from this. The integration time is not critical but should be set such that a significant response is detected, typically several orders of magnitude greater than the photodiode integration time.

7) Black-Sun Anti-blooming

A typical CMOS image sensor has a light response profile that goes from 0 dn to saturation (1023 dn for KAC-12040 in 10 bit ADC mode) and, with enough light, back to 0 dn. The sensor reaching 0 dn at very bright illumination is often called the “Black-sun” artifact and is undesirable. Black-sun artifact is typically the dominant form of anti-blooming image distortion. For the KAC-12040 the Black-sun artifact threshold is measured at the onset of saturation distortion, not at the point where the output goes to 0 dn. To first order the onset of black-sun artifact for the KAC-12040 is not proportional to the integration time or readout time.

The sensor is placed in the dark at unity gain and illuminated with a 532 nm laser with the intensity of about 26 W/cm^2 at the center of the sensor. The laser is strong enough to make the center of the laser spot below 1020 dn without any ND filters. ND filters are added to adjust the laser intensity until the signal in the region at the center of the spot increases to >1020 dn.

This illumination intensity at this ND filter is recorded (W/cm^2) as the Black-Sun Anti-blooming.
The ‘xIlumSat’ unit is calculated using and integration time of 100 µsec.

Exposing the sensor to very strong illumination for extended periods of time will permanently alter the sensor performance in that localized region.

8) Read Noise

This test is performed with no illumination and one line of integration time. The read noise is defined as one standard deviation of the frequency histogram containing the values of all pixels after the excessively deviant pixels (± three standard deviations) are removed.

9) Column Noise

After all rows are averaged together. Shading (low frequency change wrt column address) is removed. A frequency histogram is constructed of the resulting column values. The column noise is the standard deviation of the frequency histogram of the column values.

10) Row Noise

All columns are averaged together. Shading (low frequency change wrt row address) is removed. A frequency histogram is constructed of the resulting row values. The row noise is the standard deviation of the frequency histogram of the row values.

11) Maximum Photoresponse Non-Linearity

The photoresponse nonlinearity is defined as the deviation from the best fit of the sensor response using 70% of saturation and zero signal as the reference points. The different signal levels are determined by varying the integration time. The sensor saturation level is (1023-dark offset). The dark offset is subtracted from the image for the following Mavg and Lavg.

- The integration time is varied until the integration time required to reach the 70% saturation is determined. Mavg = the active array mean at the 70% saturation integration time.
- The integration is set to 1/14 (5% exposure point). Lavg = meant at the 5% exposure point
- PRNL (@ 5% saturation) =((Lavg/Mavg) * (14/1) -1) * 100

12) Maximum Gain Difference Between Outputs

The sensor contains two ADC and four channels of analog data in its highest frame rate configuration. The sensor is factory calibrated to reduce the gain differences between the channels. The gain variations are manifest as a row oriented pattern where every other row uses a different ADC. Using triple scan read out mode, an additional two analog channels are introduced resulting in a four row pattern. With one channel ('Top Ping') used as the reference, the residual gain difference is defined as:

((Bottom Ping Row Average/Top Ping Row Average) -1) * 100

((Top Pong Row Average/Top Ping Row Average) -1) * 100

((Bottom Pong Row Average/Top Ping Row Average) -1) * 100

13) Photodiode Dark Current

The photodiode dark current is measured in rolling shutter read out mode using 105 msec integration time and an analog gain = 8. The value is converted to electrons/pix/sec using the formula:

Photodiode dark current = average signal (DN) * el-per-DN (gain=8) / .105 seconds

where 'average signal (DN)' is the average of all pixels in the sensor array, and 'el-per-DN(gain=8)' is measured on each sensor using the photon transfer method.

14) Storage Node Dark Current

The storage node dark current is measured in global shutter read out mode using a special timing mode to prevent the photodiode dark current from being transferred to the storage node. In global shutter mode, the integration time of the storage node is the time it takes to read out a frame. The sensor analog gain is set to 2:

Storage node dark current = average signal (DN) * el-per-DN (gain=2) / .0138 seconds

where 'average signal (DN)' is the average of all pixels in the sensor array and 'el-per-DN(gain=2)' is measured on each sensor using the photon transfer method.

15) Lag

Lag is measured as the number of electrons left in the photodiode after readout when the sensor is illuminated at 70% of Photodiode Charge Capacity.

Analog gain is set to 8. With no illumination a 64 average dark image is recorded (Dark_ref). The 'el-per-DN' is measured using the photon transfer method.

Illumination is adjusted blink every other frame such that the mean image output is 70% of the Photodiode Charge Capacity for even frames, and with no illumination for odd frames. A 64 frame average of Odd Dark Frames is recorded as Dark_Lag.

Lag = (Dark_Lag - Dark_Ref) * el-per-DN' Units: electrons rms

16) Photodiode Charge Capacity

The sensor analog gain is reduced to <1 to prevent ADC clipping at 1023 dn. The 'el-per-DN' is measured using the photon transfer method. The sensor is illuminated at a light level ~1.5x the illumination at which the pixel output no longer linearly changes with illumination level. The Photodiode Charge Capacity is equal to the average signal (DN) * el-per-DN. Units: electrons rms.

17) Dark Field Faint Column/Row Defect

A 4 frame average, no illumination image is acquired at one line time of integration. Major defective pixels are removed (> 5 Sigma). All columns or rows are averaged together. The average of the local ROI of 128 columns or rows about the column/row being tested is determined. Any columns/rows greater than the local average by more than the threshold are identified.

18) Bright Field Faint Column/Row Defect

A 4 frame average, 70% illumination image is acquired at one line time of integration. Major defective pixels are removed (> 5 Sigma). All columns or rows are averaged together. The average of the local ROI of 128 columns or rows about the column/row being tested is determined. Any columns/rows greater than the local average by more than the threshold are identified.

19) Total Pixelized Noise

This test is performed with no illumination and one line of integration time. A single image is captured including both Temporal and Fixed Pattern Noise (FPN). A spatial low pass filter is applied to remove shading and deviant pixels (± three standard deviations) are removed. The Total Pixelized Noise is defined as one standard deviation of the frequency histogram.

20) Responsivity ke/lux-sec

This number is calculated by integrating the multiplication of the sensor QE by the human photopic response assuming a 3200K light source with a QT100 IR filter. This is a sharp 650nm cutoff filter. If the IR filter is removed a higher response value will result.

21) Responsivity V/lux-sec

Voltage levels are not output from the sensor. This metric uses the pixel output in volts at the ADC input for 1x Analog Gain.

Operation

This section is a brief discussion of the most common features and functions assuming default conditions. See the *KAC-12040 User Guide* for a full explanation of the sensor operation modes, options, and registers.

Register Addresses

The last bit of any register address is a Read/Write bit. Most references in this document refer to the Write address. All SPI reads are to an even address, all SPI writes are to an odd address.

Sensor States

Figure 11 shows the sensor states, see the *KAC-12040 User Guide* for detailed explanation of the States.

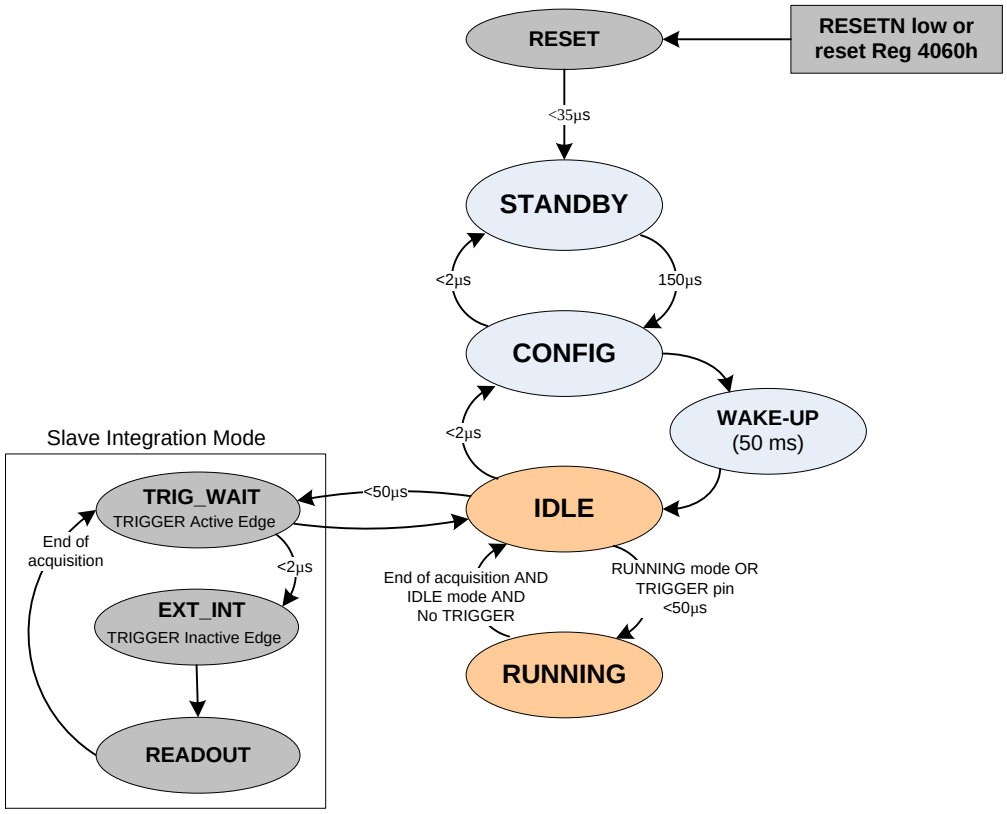


Figure 11: Sensor State Diagram

ENCODED SYNCS

To facilitate system acquisition synchronization the KAC-12040 places synchronization words (SW) at the beginning and at the end of each output row as indicated in the following Figure 12. This is performed for each of the 8 LVDS output banks providing frame, line, and output synchronization. See the *KAC-12040 User Guide* for additional detail on LVDS and Encoded Sync output.

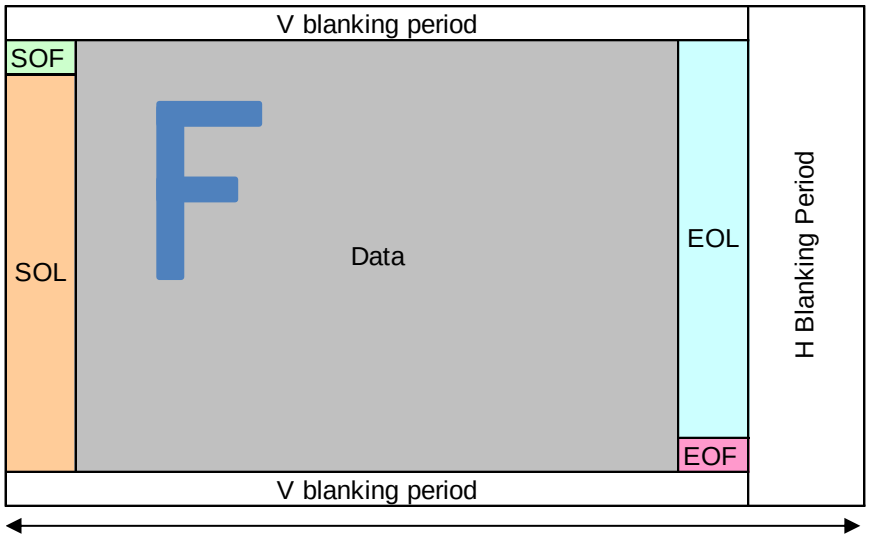


Figure 12: Encoded Frame Syncs

LINE TIME

This Datasheet presumes the recommended startup script that is defined in the *KAC-12040 User Guide* has been applied. The KAC-12040 defaults to Dual-Scan mode. In this mode the LVDS data readout overlaps the pixel readout and ADC conversion time. The Pixel and ADC conversion time are fixed (for 10 bit operation) and total ~ 8.66 µsec. The LVDS time will be dependent on the PLL2 frequency selected. If the PLL2 < 313 MHz, then the LVDS data readout will dominate the row time. For PLL2 > 313 MHz, the Pixel + ADC will set the minimum Line Time. The Line Time is not impacted by the selection of Rolling Shutter or Global Shutter mode.

The KAC-12040 architecture always outputs two rows at once, one row from the top ADC, and one from the bottom ADC. Each ADC then divides up the pixel into 1 → 4 parallel pixel output LVDS Banks. The default is 4 output banks per ADC for a total of 8 parallel pixel outputs to minimize the LVDS data output time. Since the sensor always outputs 2 rows at a time the timing and registers are based on a Line Time (LT) or Line Length (LL) where one LT = the time to readout 2 rows in parallel (one even row and one odd row).

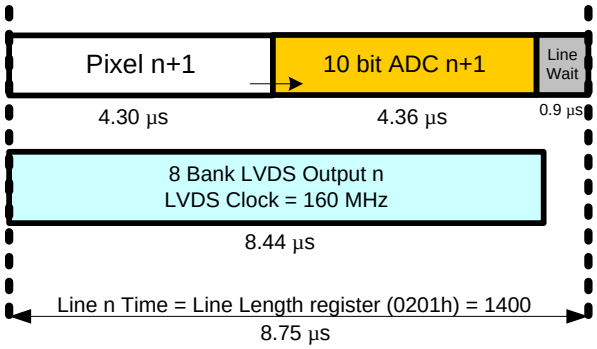


Figure 13: Default Line Time (Dual-Scan) with PLL2 = 320 MHz

FRAME TIME

The frame time is defined in units of Line Time. 1 Line Time unit = 2 output rows. To first-order the frame rate is not directly impacted by selection of Global Shutter, Rolling Shutter, Dual-Scan, or Tri-Scan.

The Frame Time is made up of three phases:

1. Integration Phase
2. Readout Phase
3. Frame Wait Phase (Vertical Blanking, Vblank)

By default the Integration Phase overlaps the Readout and Frame Wait Phases. If the Integration Phase is larger than the Readout + Frame Wait time, then the Integration Phase will determine the video frame rate. Otherwise the frame rate will be set by the Readout + Frame Wait time. In other words, if the programmed integration time is larger than the minimum readout time (and vertical blanking) then extra vertical blanking will be added and the frame rate will slow to accommodate the requested integration time.

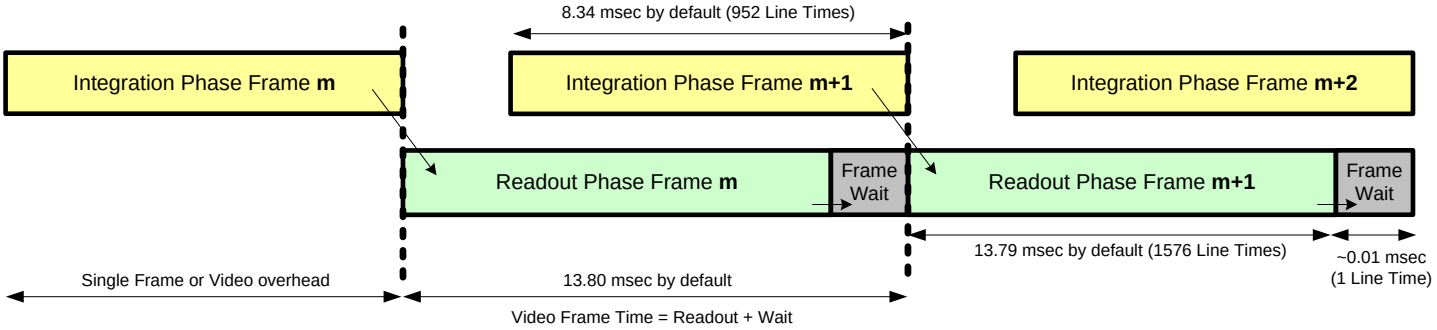


Figure 14: Default frame time configuration (Frame A)

If the Integration Phase is less than the Readout Phase then the start of integration is automatically delayed to minimize the storage time and dark current.

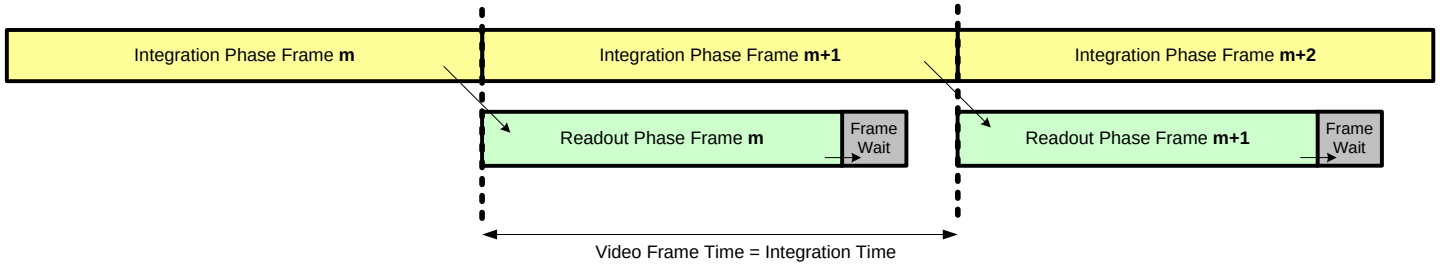


Figure 15: Frame time with extended integration time.

If the Readout Phase(+ Vblanking) is less than the Integration Phase, then the readout occurs as soon the integration is complete to minimize the storage time and dark current.

See the *KAC-12040 User Guide* for detailed calculation of the Integration Phase, Readout Phase, and Frame Wait.

To first-order the Readout Phase is equal to the number of rows * row_time.

GLOBAL SHUTTER READOUT

Global Shutter readout provides the maximum precision for freezing scene motion. Any motion artifacts will be 100% defined by an ideal integration time edge. Every pixel in the array starts and stops integration at the same time.

Figure 16 illustrates a Global Shutter Frame readout assuming the recommended Start-up Script defined in the *KAC-12040 User Guide* (8 LVDS banks, Dual-Scan, 8.75 µSec line time). The Frame Wait Phase is not shown due to its small default size (1 LL) and for clarity.

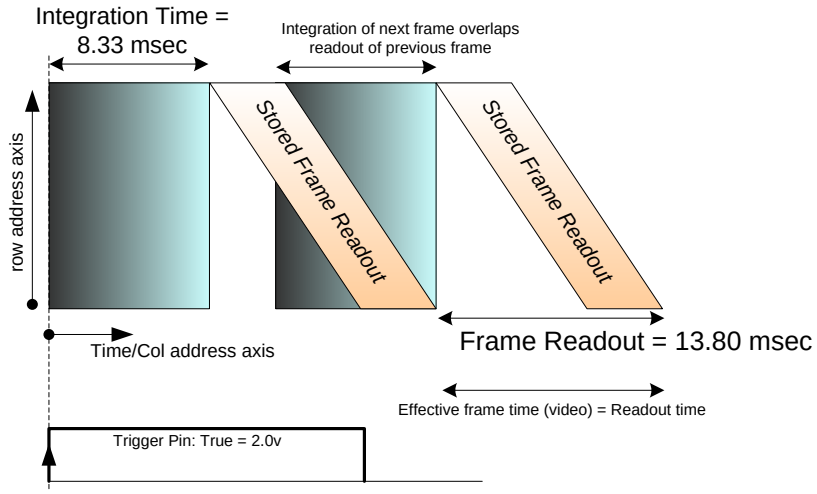


Figure 16: Illustration of frame time for Global Shutter readout

Global Shutter readout mode is selected using Bits [1:0] of Register 01D1h.

Images can be initiated by setting and holding the TRIGGER input pin or by placing the sensor into RUNNING mode by writing 03d to register 4019h. If the TRIGGER input pin is true when at the start of the integration time for the next frame then the sensor will complete an additional frame integration and readout. In the case shown in Figure 16 two frames will be output.

ROLLING SHUTTER READOUT

The KAC-12040 high speed Rolling Shutter readout provides the maximum dynamic range while still providing excellent motion capture. In Rolling Shutter the readout more closely matches a film camera shutter. Each row of the image receives the same integration time, but each row starts and ends at a different time as the shutter travels from the top of the array to the bottom. In the Figure 17 frame time illustration this 'moving shutter' displays as a sloped edge for the blue pixel array region, just as the readout edge is sloped.

The Figure 17 illustration shows a 2 frame output sequence using the external TRIGGER pin.

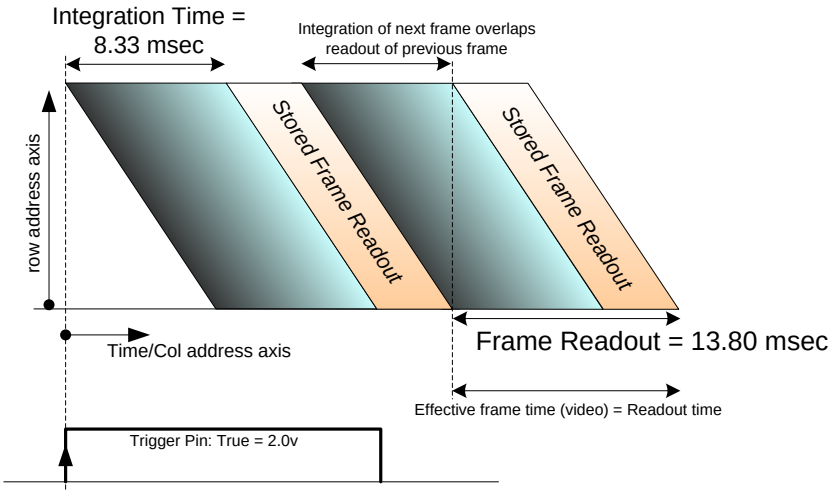


Figure 17: Illustration of Frame time for Rolling Shutter readout

Rolling Readout mode can be selected using Bits [1:0] of Register 01D1h.

Images can be initiated by setting and holding the TRIGGER input pin or by placing the sensor into RUNNING mode by writing 03d to register 4019h. If the TRIGGER input pin is True when at the start of the integration time for the next frame then the sensor will complete an additional frame integration and readout.

8 Bank LVDS Data Readout

LVDS Banks

The KAC-12040 provides 8 parallel pixel banks, each consisting of 8 LVDS differential pairs (7 data pairs + 1clock pair). This allows the output of 8 pixels per LVDS clock period. All 7 data pairs, of each bank, are used only in 14 bit operation mode. By default only 5 data pairs are used for 10 bit mode (D4 –> D0). The unused pairs are held in low-power high impedance mode.

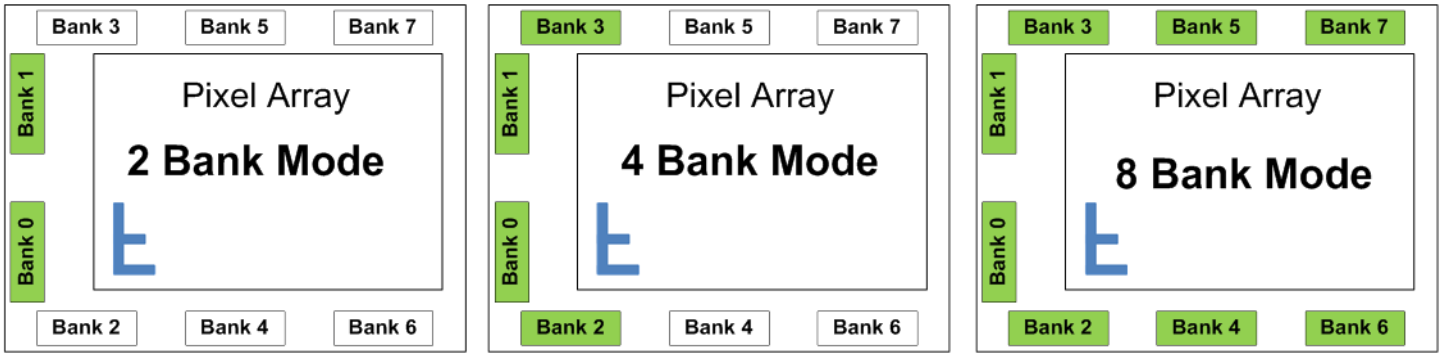


Figure 18: LVDS Bank labeling

The number of output banks used is independent of the ADC bit depth chosen. By default the KAC-12040 uses all 8 output banks for maximum frame rate. If technical restrictions prevent the use of 8 LVDS banks, the sensor can be programmed to use 4 or 2 banks, however this can result in reduced frame rate and reduction of image quality. It is recommended that 8 banks be used when possible. Only the 8 bank option is discussed in detail in this specification, see the *KAC-12040 User Guide* for additional detail on 4 and 2 bank mode.

In order to minimize the LVDS clock rate (and power) for a given data rate the pixels are output in DDR (Double Data Rate) where the MSB is always sent first (on rising edge) and the LSB second (falling edge) This is not programmable.

Ports per LVDS Bank

The MSB comes out first on the falling edge, followed by the LSB on the net rising edge.

Bit Depth	Edge of DATA_CLK	Data0	Data1	Data2	Data3	Data4	Data5	Data6
14 bits	Falling (MSB nibble)	D7	D8	D9	D10	D11	D12	D13
	Rising (LSB nibble)	D0	D1	D2	D3	D4	D5	D6
12 bits	Falling (MSB nibble)	D6	D7	D8	D9	D10	D11	HiZ
	Rising (LSB nibble)	D0	D1	D2	D3	D4	D5	HiZ
10 bits	Falling (MSB nibble)	D5	D6	D7	D8	D9	HiZ	HiZ
	Rising (LSB nibble)	D0	D1	D2	D3	D4	HiZ	HiZ
8 bits	Falling (MSB nibble)	D4	D5	D6	D7	HiZ	HiZ	HiZ
	Rising (LSB nibble)	D0	D1	D2	D3	HiZ	HiZ	HiZ

Figure 19: Number of LVDS pairs (ports) used vs. bit depth

8 Bank Pixel Order

The KAC-12040 always processes two rows at a time. Even row decodes are sent to the bottom ADC and LVDS output banks (0, 2, 4, 6). Odd rows are sent to the top ADC and LVDS banks (1, 3, 5, 7). The ROI must be (and is internally forced to) an even size and always starting on an even row decode.

The rows are read out progressively left to right (small column address to large). Eight pixels are sent out of the chip at once, one pixel per LVDS bank per LVDS clock cycle.

Pixel Readout order:

1. Two rows are selected, the even row is sent to the bottom ADC and the odd row to the top ADC.
2. Each ADC converts its row of pixel data at once and stores the result in a line buffer.
3. At default settings there are 4 output LVDS banks for each ADC.
4. Each LVDS Bank outputs one pixel per clock cycle, so 4 pixels of each row are output each full LVDS clock cycle, two rows in parallel for 8 pixels per clock cycle total.
5. The pixels are sent out from left to right (low column number to high column number). So the first 4 pixels are sent out on clock cycle 1, and the next 4 pixels to the right are sent out on clock cycle 2.
6. To conserve the number of wires per port, the 10 bits per pixel are sent out DDR (Dual Data Rate) over 5 ports. On the falling edge the upper 5 MSB bits are sent out, and on the rising edge the lower 5 bits LSB are sent out. Completing one full LVDS clock cycle and one set of eight pixels.

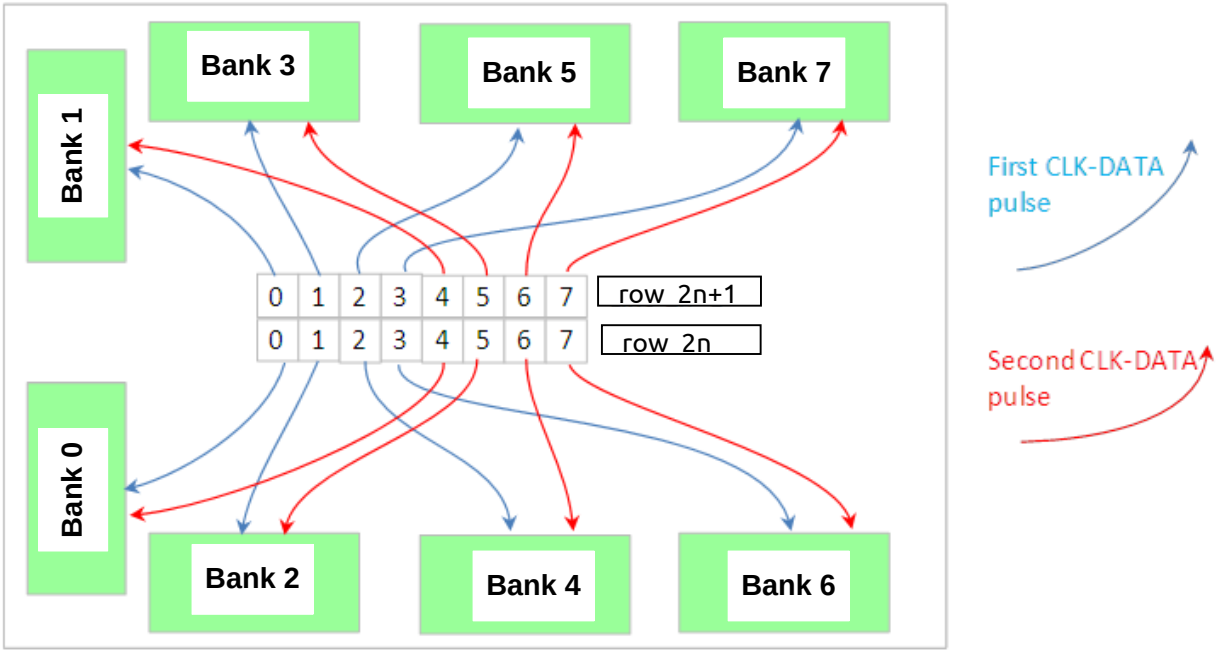


Figure 20: Pixel readout order diagram

LVDS Bank	Row	Pixel number				
Bank 0	2 n (even)	0	4	8	12	16
Bank 2	2 n (even)	1	5	9	13	17
Bank 4	2 n (even)	2	6	10	14	18
Bank 6	2 n (even)	3	7	11	15	19
Bank 1	2 n+1 (odd)	0	4	8	12	16
Bank 3	2 n+1 (odd)	1	5	9	13	17
Bank 5	2 n+1 (odd)	2	6	10	14	18
Bank 7	2 n+1 (odd)	3	7	11	15	19
	LVDS Clock Cycle	1	2	3	4	5

Figure 21: Pixel readout order table

DE-SERIALIZER SETTINGS

Figure 22 shows the data stream of one LVDS bank for 10 bit resolution.

Data serialization is fixed at 2 cycle DDR for all bit depths. Data output order is MSB first on the falling edge, and LSB following on the rising edge.

Four pixel values per synchronization word are embedded into the video stream per LVDS bank.

The SOL/SOF synchronization words are sent out of each LVDS bank before the first valid pixel data from that bank. Each bank outputs all 4 syncs of the SOF or SOL.

And each of the active LVDS banks each output all 4 sync codes for the EOL/EOF.

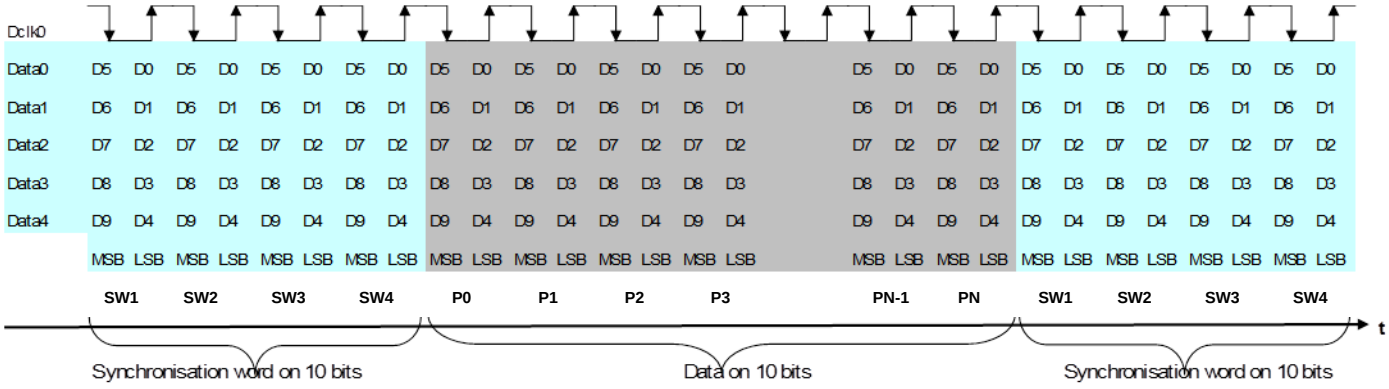


Figure 22: Data stream of one LVDS Bank for 10bits ADC resolution

Register Definition

16 bit Write addr (Hex)	Default Value Hex/Dec	SPI State	Group	Register Name
0001	420d	Any	Frame A Definition	Frame A ROI y1
0009	2176d			Frame A ROI h1
0011	80d			Frame A ROI x1
0019	3856d			Frame A ROI w1
0021	0d			Frame A sub-ROI y2
0029	0d			Frame A sub-ROI h2
0031	0d			Frame A sub-ROI x2
0039	0d			Frame A sub-ROI w2
0041	0d			Frame A sub-ROI y3
0049	0d			Frame A sub-ROI h3
0051	0d			Frame A sub-ROI x3
0059	0d			Frame A sub-ROI w3
0061	0d			Frame A sub-ROI y4
0069	0d			Frame A sub-ROI h4
0071	0d			Frame A sub-ROI x4
0079	0d			Frame A sub-ROI w4
0081	0033h			Frame A Decimation
0089	0d			Frame A Video Blanking
0091	800d			Frame A Integration Lines
0099	0d			Frame A Integration Clocks
00A1	10d			Frame A Black Level
00A9	001Fh			Frame A Gain
00E9	0d	Any	Frame B Definition	Frame B ROI y1
00F1	3016d			Frame B ROI h1
00F9	0d			Frame B ROI x1
0101	4016d			Frame B ROI w1
0109	0d			Frame B sub-ROI y2
0111	0d			Frame B sub-ROI h2
0119	0d			Frame B sub-ROI x2
0121	0d			Frame B sub-ROI w2
0129	0d			Frame B sub-ROI y3
0131	0d			Frame B sub-ROI h3
0139	0d			Frame B sub-ROI x3
0141	0d			Frame B sub-ROI w3
0149	0d			Frame B sub-ROI y4
0151	0d			Frame B sub-ROI h4
0159	0d			Frame B sub-ROI x4
0161	0d			Frame B sub-ROI w4
0169	0033h			Frame B Decimation
0171	0d			Frame B Video Blanking
0179	800d			Frame B Integration Lines
0181	0d			Frame B Integration Clocks
0189	10d			Frame B Black Level
0191	001Fh			Frame B Gain

16 bit Write addr (Hex)	Default Value Hex/Dec	SPI State	Description
01D1	CC11h	CONFIG only	Config1
01D9	0000h	CONFIG or IDLE	Config2
01E1	000Ah	CONFIG or IDLE	Analog/Digital Power Mode
01E9	0000h	CONFIG or IDLE	Dual-Video Repetition
01F1	0d	CONFIG or IDLE	Vertical Blanking
01F9	1938d	CONFIG or IDLE	Fixed Frame Period
0201	1376d	CONFIG or IDLE	Line Length (LL)
0209	0028h	CONFIG or IDLE	ADC Bit Depth
0211	0000h	CONFIG or IDLE	FLO Edge
0219	0000h	CONFIG or IDLE	MSO Edge
0709	0000h	Any	CFA Feedback
0711	0000h	Any	Temperature Sensor FB
0719	0000h	Any	General Feedback
2059	0300h	CONFIG only	Output Bank Select 1
2099	2877h	CONFIG only	PLL1 Setting
20A1	0861h	CONFIG only	PLL2 Setting
2449	0432h	CONFIG only	Sub-LVDS Enable
2479	10ABh	Any	Column Clamp Threshold A
2481	20C7h	Any	Column Clamp Threshold B
2499	0011h	CONFIG or IDLE	Test Pattern Control 1
24A1	0220h	CONFIG or IDLE	Test Pattern Control 2
24B9	202d	STANDBY only	Slope 1 Length
24C1	101d	STANDBY only	Slope 2 Length
24C9	101d	STANDBY only	Slope 3 Length
24D1	101d	STANDBY only	Slope 4 Length
24D9	101d	STANDBY only	Slope 5 Length
24E1	420d	STANDBY only	Slope 6 Length
24E9	0083h	STANDBY only	Slope 1/2 Gain
24F1	038Fh	STANDBY only	Slope 3/4 Gain
24F9	0FBFh	STANDBY only	Slope 5/6 Gain
2501	1F9Fh	STANDBY only	Slope 7 Gain
2559	4804h	Any	Defect Avoidance Threshold
2561	0006h	Any	Defect Avoidance Enable
25C1	0003h	CONFIG or IDLE	Encoded Sync Config
25C9	000Ah	CONFIG only	LVDS Power-Down
2619	000Bh	CONFIG only	Output Bank Select 2
2D89	0000h	CONFIG only	FLO/MSO Polarity
4001	4100h	Any	Chip Revision Code
4009	0011h	Any	Chip ID Code MSB
4011	0080h	Any	Chip ID Code LSB
4019	0000h	Any	Set Sensor State
4021	0000h	CONFIG or IDLE	OTP Address
4029	0000h	CONFIG or IDLE	OTP Write Data
4031	0000h	CONFIG or IDLE	Command_Done_FB
4041	0000h	CONFIG or IDLE	OTP Read Data
4061	0000h	CONFIG or IDLE	Soft Reset

Notes – SPI State (the Sensor State from which the register can be set):

1. "Any": Can be written from any state (including RUNNING)
2. "CONFIG or IDLE": These registers can be changed in IDLE or CONFIG states
3. "CONFIG only": Sensor must be in CONFIG state to set these registers.
4. Only Register 4018h and 4060h may be set when the sensor is in STANDBY state.

Notes - Decimal, hexadecimal, binary values:

1. "b" denotes a binary number, a series of bits: MSB is on the left, LSB is on the right.
2. "h" or "hex" denotes a hexadecimal number (Base 16, 1-9, A-F). The letters in a hex number are always capitalized
3. "d" denotes a decimal number.
4. Note that "0" and "1" are the same value in all number base systems and sometimes the base notation is omitted.

The KAC-12040 features an embedded microprocessor by Cortus.

Absolute Maximum Ratings

For Supplies and Inputs the maximum rating is defined as a level or condition that should not be exceeded at any time. If the level or the condition is exceeded, the device will be degraded and may be damaged. Operation at these values will reduce Mean Time to Failure (MTTF).

SUPPLIES

Parameter	Value
AVDD_LV, VDD_DIG	-0.25 V; 2.3 V
AVDD_HV, Vref_P, VDD_LVDS	-0.25 V; 4 V
DC Input voltage at any input pin	-0.25 V; VDD_DIG +0.25 V

CMOS INPUTS

Parameter	Symbol	Min	Typical	Max	Unit
Input voltage low level	V_{IL}	-0.3		0.35 VDD_DIG	V
Input voltage high level	V_{IH}	0.65 VDD_DIG		VDD_DIG +0.3	V

Operating Ratings

Input Clock Conditions

Parameter	Min	Typical	Max	Unit
Frequency for Clk_In1 and Clk_In2	45	48	50	MHz
Duty cycle for Clk_In1 and Clk_In2	40	50	60	%
RESETN	10			ns
TRIGGER pin minimum pulse width	20			ns

TRIGGER must be active at least 4 periods of PLL1 (~12.5 ns at 320 MHz) to start a capture cycle. The polarity of the active level is configurable by SPI (Register 01D8h Bit 0), the default is active high (ie pin = VDD_DIG = trigger request).

Operating Temperature

Description	Symbol	Minimum	Maximum	Units	Notes
Operating Temperature	TOP	-50	+80	°C	1

Notes:
1. Under conditions of no condensation on the sensor

CMOS IN/OUT

CMOS IN/OUT characteristics

Parameter	Symbol	Min	Typical	Max	Unit
Output voltage low level	V_{OL}			0.45	V
Output voltage high level	V_{OH}	VDD_DIG–0.45			V
Input Hysteresis voltage	V_{TH}		0.25		
Pull-up resistor value for RESETN pin	R_{PU}	62			kΩ
Pull-down resistor value for TRIGGER pin	R_{PD}	100			kΩ
Current on ADC_REF pin	I_{ADC_REF}		100		µA

SUPPLIES

Parameter	Symbol	Min	Typical	Max	Unit	Comment
LVDS IO supply	VDD_LVDS	3.15	3.30	3.63	V	
Pixel high voltage supply	AVDD_HV	3.40	3.50	3.60	V	
Pixel low voltage supply	Vref_P	2.71	2.80	2.88	V	
Analog power supply	AVDD_LV	1.71	1.80	1.89	V	
Digital power supply	VDD_Dig	1.9	2.00	2.10	V	
AVDD_HV – Vref_P			0.5		V	
Power in STANDBY State			10		mW	
Current in STANDBY State						
VDD_LVDS			< 0.5		mA	
AVDD_HV			< 0.5		mA	
AVDD_LV			< 0.5		mA	
Vref_P			< 0.5		mA	
VDD_DIG			4		mA	
Power in CONFIG State			330		mW	
Current in CONFIG State						
VDD_LVDS			< 0.5		mA	
AVDD_HV			< 0.5		mA	
AVDD_LV			< 0.5		mA	
Vref_P			< 0.5		mA	
VDD_DIG			145		mA	
Power in IDLE State			410		mW	
Current in IDLE State						
VDD_LVDS			< 0.5		mA	
AVDD_HV			20		mA	
AVDD_LV			< 0.5		mA	
Vref_P			< 0.5		mA	
VDD_DIG			145		mA	
Power in RUNNING State			1.5		W	
Current in RUNNING State						
VDD_LVDS in standard LVDS mode			164		mA	
VDD_LVDS in Sub-LVDS mode			104		mA	
AVDD_HV			74		mA	
AVDD_LV			12		mA	
Vref_P			26		mA	
VDD_DIG			396		mA	

Notes:

1. Voltages relative to VSS. Current measurements made in darkness.
2. PLL2 = 320 MHz, Max frame rate (i.e., no row or frame wait time). These average power values will decrease at lower frame rate either from reduced PLL2 or low power state during Line and Frame blanking.
3. Sub-LVDS active.

SPI (Serial Peripheral Interface)

The SPI communication interface lets the application system to control and configure the sensor. The sensor has an embedded slave SPI interface. The application system is the master of the SPI bus.

Name	Sensor I/O direction	Description
CSN	I	SPI chip select - Active low, this input activates the slave interface in the sensor
SCK	I	SPI clock – toggled by the master
MISO	O	SPI master serial data input – slave(sensor) serial data output
MOSI	I	SPI master serial data output – slave(sensor) serial data input

Parameter	Min	Typ	Max	Unit
SPI SCK	5	25	50	MHz
Duty cycle on SPI SCK	40	50	60	%

Clock Polarity and Phase

CPOL(Clock POLarity) and CPHA(Clock PHAse) are commonly defined in SPI protocol such as to define SCK clock phase and polarity. The KAC-12040 defaults to expecting the master to be configured with CPOL=1 (the base value of the clock is VDD_DIG) and CPHA=1 (data is valid on the clock rising edge).

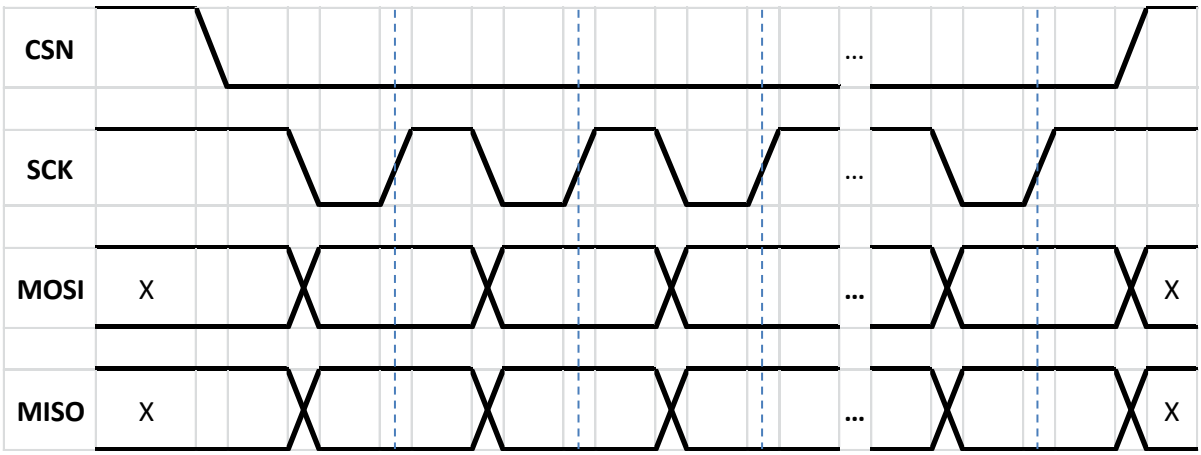


Figure 23: CPOL = 1 and CPHA = 1 configuration

SPI PROTOCOL

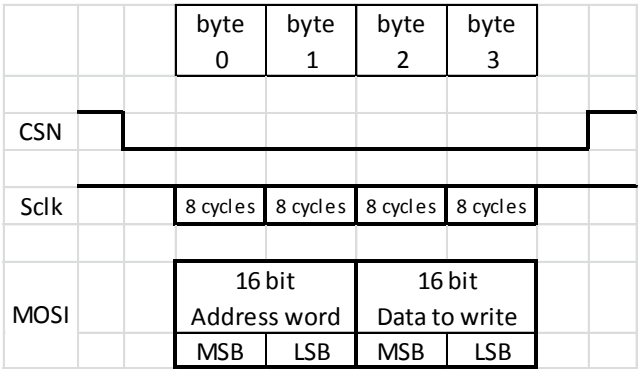


Figure 24: SPI Write byte order

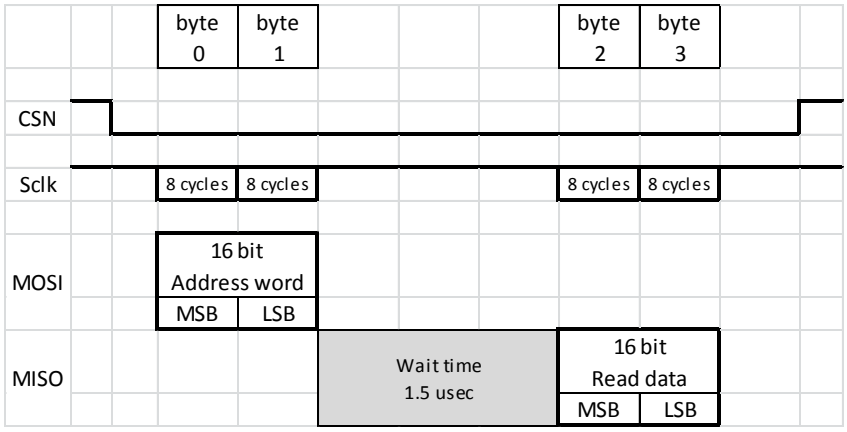


Figure 25: SPI Read byte order

There is a delay during readback between presenting the address to be read on the MOSI and being able to read the register contents on the MISO. This delay is not the same for all registers. Some are available immediately, some require a longer fetch time. The 1.5 µsec shown in Figure 14 is the maximum time to fetch a register's value when in CONFIG state (the recommended state for changing registers). Some registers can be adjusted during RUNNING state (see the register summary on page 34). If performing a readback during RUNNING state, the delay could be as long as 4.5 µsec depending on when in the row the request was sent and the sensor's microcontroller activity at that moment.

Note that readback does not provide the actual register value being used, but reflects the next value to be used. All new register writes are placed in a shadow memory until they can be updated into the active memory. This active memory update occurs at the start of the next frame or upon entering the state listed in the Register Summary table on page 34. Register reads access this shadow memory not the active memory. For instance if the sensor is in RUNNING mode and you adjust the LL in register 200h. You can read back and confirm that your register change was received by the sensor; however, the LL will not change since register 200h can only be changed in CONFIG state. If you change the sensor state to CONFIG and then back to RUNNING, then the new LL will take effect.

SPI INTERFACE

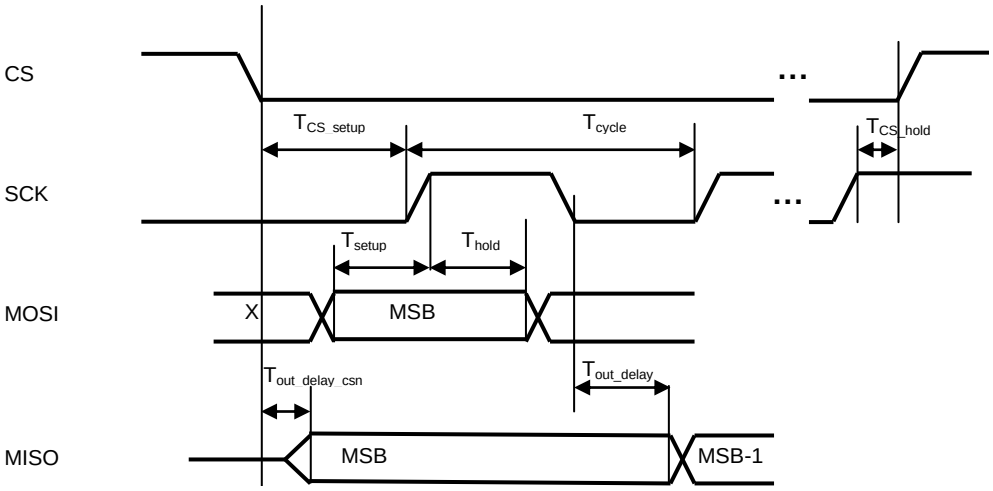


Figure 26: SPI timing chronogram

SPI TIMING SPECIFICATION

Symbol	Min Value	Max Value
T_{cycle}	20 ns	200 ns
T_{setup}		2.9 ns
T_{hold}	0.8 ns	
T_{cs_setup}		2.5 ns
T_{cs_hold}	0.1 ns	
$T_{out\_delay\_csn}$	3.1 ns	4.7 ns
T_{out_delay}	4.9 ns	8.7 ns

LVDS Interface

The data output can be configured to follow standard TIA/EIA-644-A LVDS specification or a low power mode compatible with common Sub-LVDS definition used in FPGA industry. (Please refer to the *KAC-12040 User Guide* for more information).

Unless otherwise noted, min/max characteristics are for T = -40 °C to +85 °C, output termination resistance RL = 100 Ω ± 1%, Typical values are at VDD_LVDS =3.3 V.

Use register 2449h to select standard or Sub-LVDS. This document assumes that Sub-LVDS is active for all power measurements. Standard LVDS can increase the average power consumption as much as 200 mW in the case of minimum horizontal and vertical blanking.

STANDARD LVDS CHARACTERISTICS

Parameter	Symbol	Min	Typical	Max	Unit
Differential output voltage	VOD	250	355	450	mV
VOD variation between complementary output states	ΔVOD	-20		+20	mV
Common mode output voltage	VOCM	1.235	1.259	1.275	V
VOCM variation between complementary output states	ΔVOCM	-25		+25	mV
High impedance leakage current	IOZD	-1		+1	µA
Output short circuit current: when D+ or D- connected to ground when D+ or D- connected to 3.3V	IOSD	 2.9 12.25		 4.3 30.47	mA
Output capacitance	CDO		1.3		pF
Maximum Transmission Capacitive Load Expected (for 260 MHz LVDS clock)				10	pF

SUB-LVDS CHARACTERISTICS

Parameter	Symbol	Min	Typical	Max	Unit
Differential output voltage	V_{OD}	140	180	220	mV
VOD variation between complementary output states	ΔV_{OD}	-5		+5	mV
Common mode output voltage	V_{OCM}	0.88	0.9	0.92	V
VOCM variation between complementary output states	ΔV_{OCM}	-10		+10	mV
High impedance leakage current	I_{OZD}	-1		+1	µA
Output short circuit current: when D+ or D- connected to ground when D+ or D- connected to 3.3V	I_{OSD}	 1.4 10.21		 2.2 30.47	mA
Output capacitance	C_{DO}		1.3		pF
Maximum Transmission Capacitive Load Expected (for 260 MHz LVDS clock)				10	pF

Parameter	Min	Typical	Max	Unit
LVDS_CLK	50	160	160	MHz
Duty cycle on LVDS_CLK		50		%

IN-BLOCK LVDS TIMING SPECIFICATION

The table below gives LVDS timing specification for one group of LVDS for nominal frequency of 260 MHz. There is no skew specification between groups.

Parameter	Symbol	Value	Typical	Max	Unit
Minimum time between data change and clock rising edge	ts_{DLH}	600			ps
Minimum time between clock rising edge and data change	th_{DLH}	600			ps
Minimum time between data change and clock falling edge	ts_{DHL}	600			ps
Minimum time between clock falling edge and data change	th_{DHL}	600			ps
Maximum differential skew between the 7 data pairs	t_{SKD}		200	700	ps

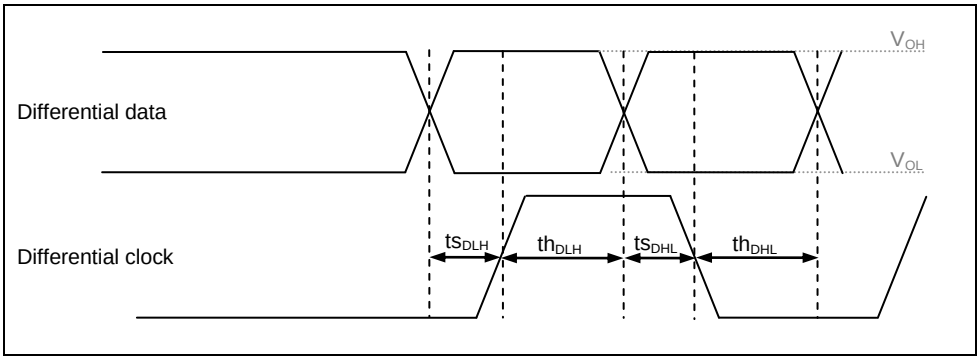


Figure 27: LVDS timing chronogram

INTER-BLOCK LVDS TIMING SPECIFICATION

Parameter	Min	Typical	Max	Unit
Inter-block skew		6	12	LVDS Clock period

Storage and Handling

Storage Conditions

Description	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	TST	-40	+80	°C	1
Humidity	RH	5	90	%	2

Notes:
1. Long-term storage toward the maximum temperature will accelerate color filter degradation.
2. T=25 °C. Excessive humidity will degrade MTTF.

ESD

1. This device contains limited protection against Electrostatic Discharge (ESD). ESD events may cause irreparable damage to an image sensor either immediately or well after the ESD event occurred. Failure to protect the sensor from electrostatic discharge may affect device performance and reliability.
2. Devices should be handled in accordance with strict ESD procedures. Devices are shipped in static-safe containers and should only be handled at static-safe workstations.
3. See Application Note *Image Sensor Handling Best Practices* for proper handling and grounding procedures. This application note also contains workplace recommendations to minimize electrostatic discharge.
4. Store devices in containers made of electro-conductive materials.

Cover Glass Care and Cleanliness

1. The cover glass is highly susceptible to particles and other contamination. Perform all assembly operations in a clean environment.
2. Touching the cover glass must be avoided.
3. Improper cleaning of the cover glass may damage these devices. Refer to Application Note *Image Sensor Handling Best Practices*.

Environmental Exposure

1. Extremely bright light can potentially harm image sensors. Do not expose to strong sunlight for long periods of time, as the color filters and/or microlenses may become discolored. In addition, long time exposures to a static high contrast scene should be avoided. Localized changes in response may occur from color filter/microlens aging.
2. Exposure to temperatures exceeding maximum specified levels should be avoided for storage and operation, as device performance and reliability may be affected.
3. Avoid sudden temperature changes.
4. Exposure to excessive humidity may affect device characteristics and may alter device performance and reliability, and therefore should be avoided.
5. Avoid storage of the product in the presence of dust or corrosive agents or gases, as deterioration of lead solderability may occur. It is advised that the solderability of the device leads be assessed after an extended period of storage, over one year.

Soldering Recommendations

1. For manual soldering the soldering iron tip temperature is not to exceed 370 °C. Higher temperatures may alter device performance and reliability.
2. Re-Flow soldering method is not recommended. Wave soldering may be employed, however solder should not touch the cover glass.

Mechanical Information

COMPLETED ASSEMBLY

Notes:

1. See Ordering Information for marking code.
2. No materials to interfere with clearance through package holes.
3. Imaging Array is centered at the package center.
4. Length dimensions in mm units

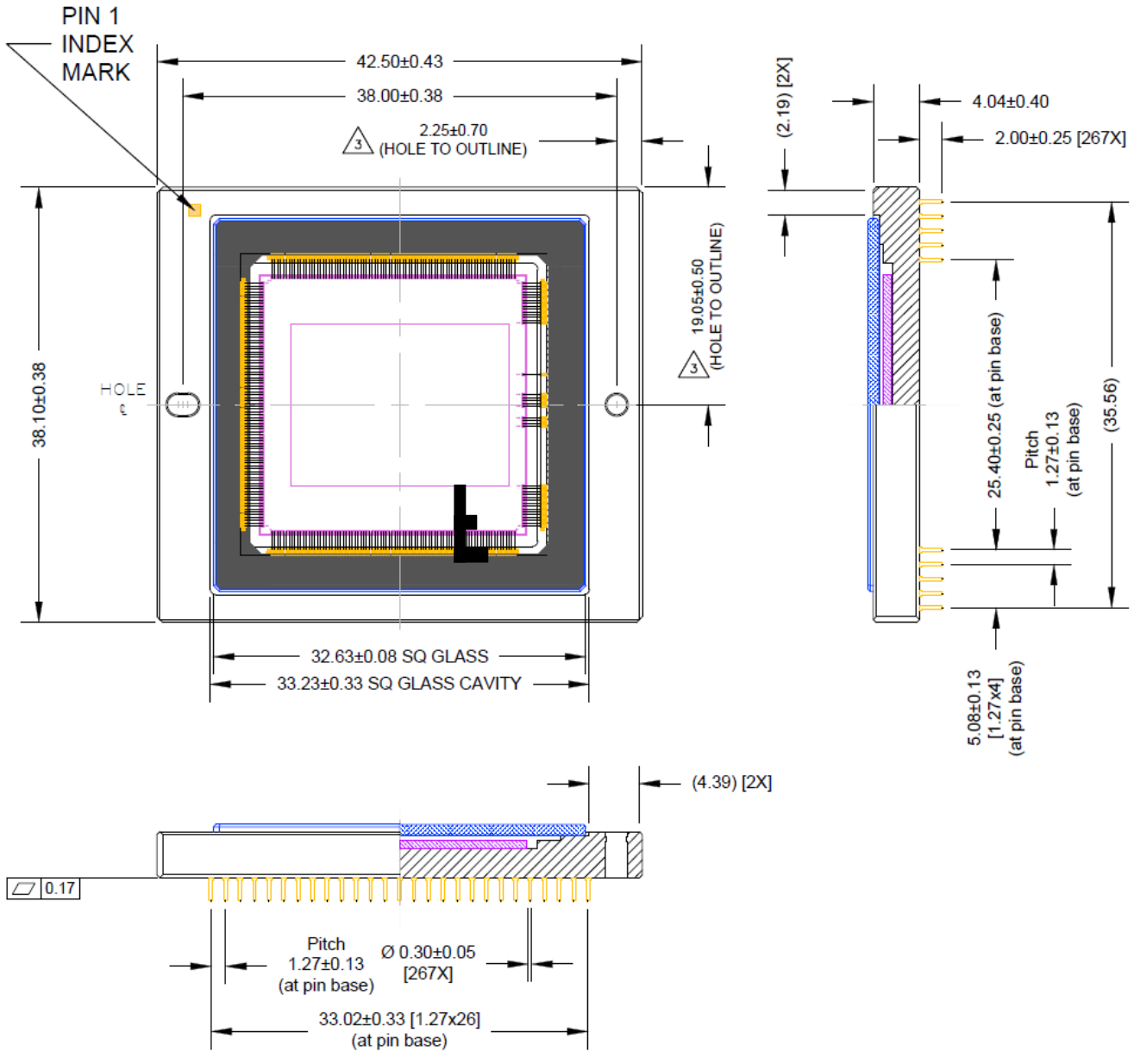


Figure 28: Completed Assembly (1 of 5)

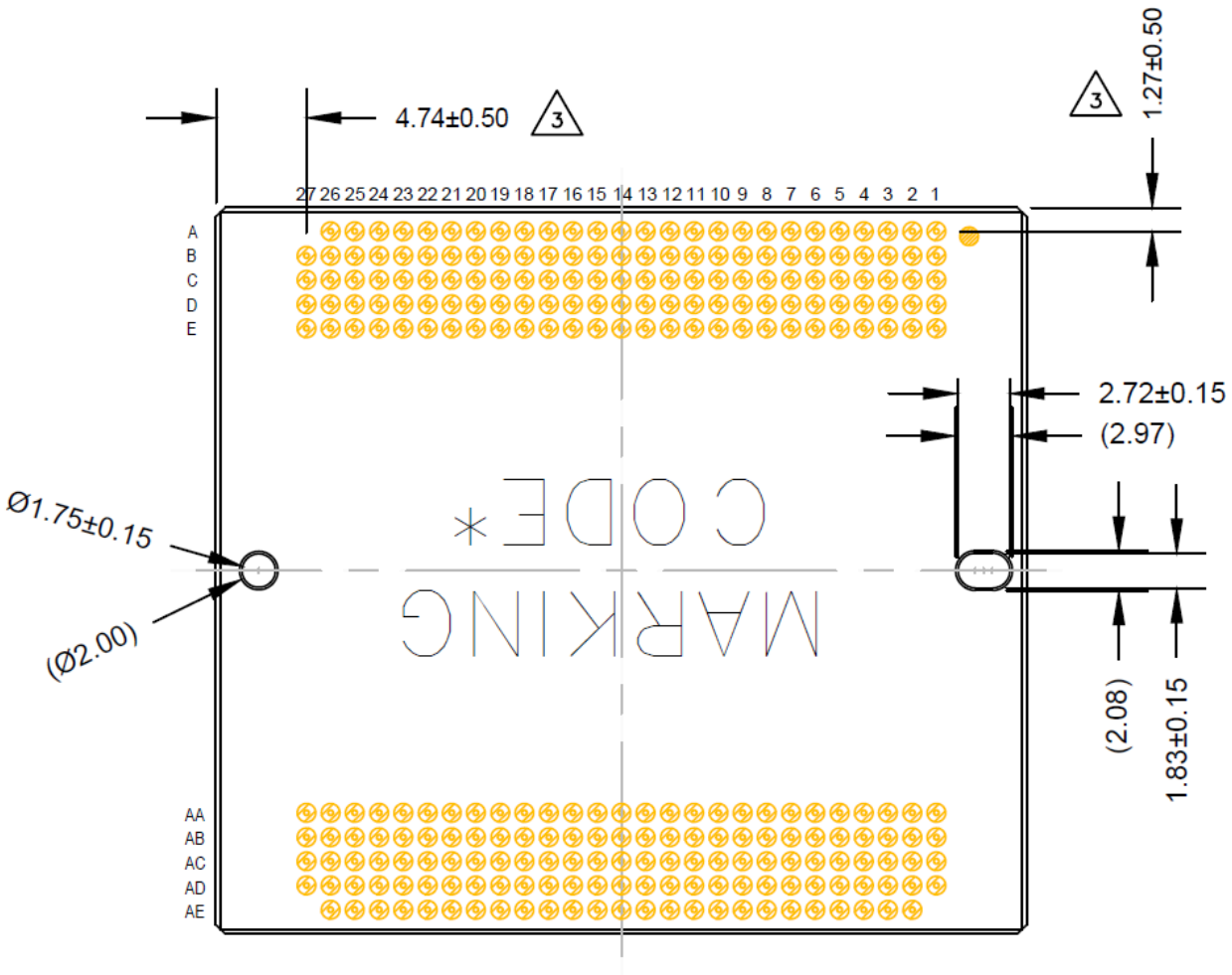


Figure 29: Completed Assembly (2 of 5)

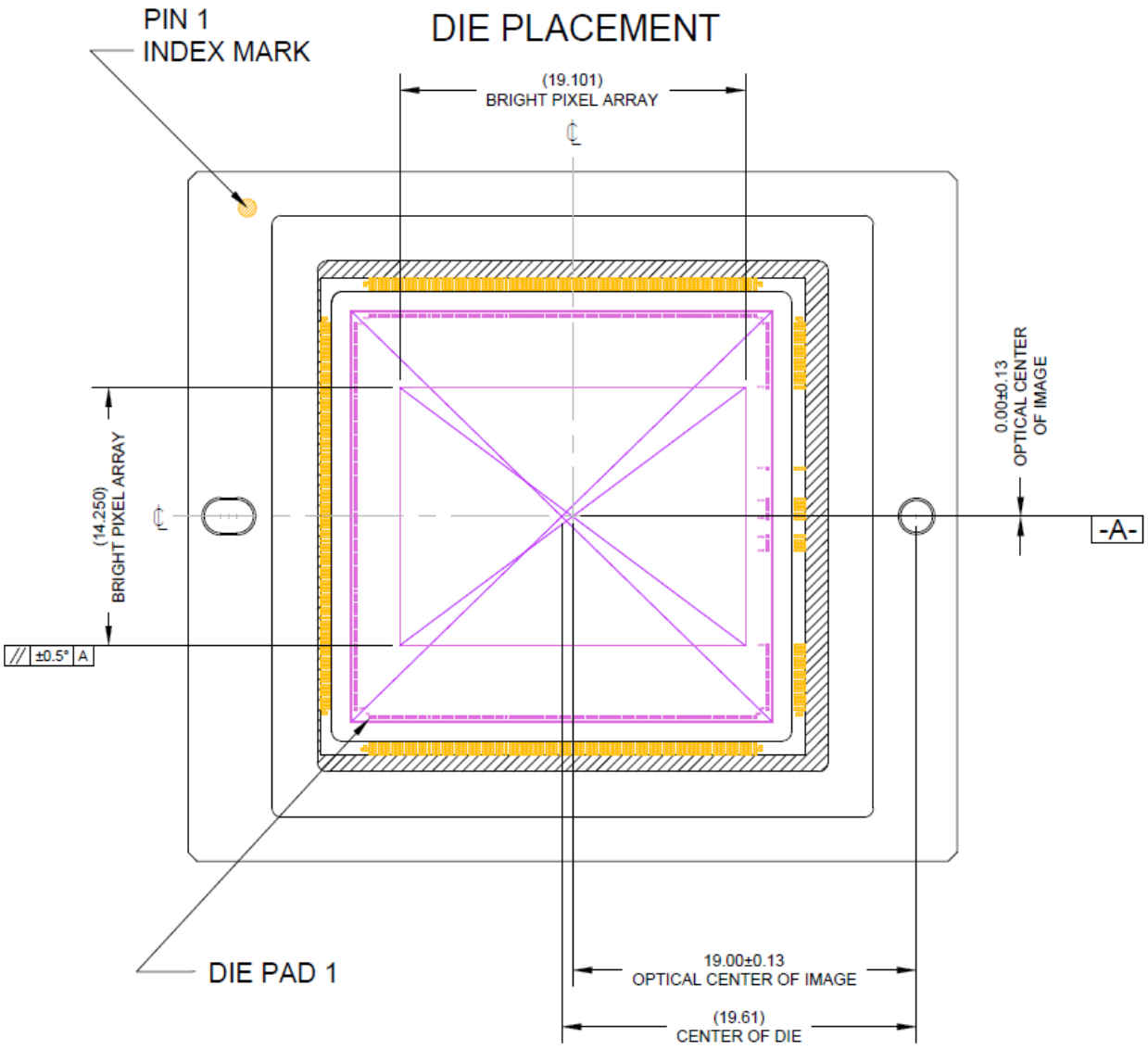


Figure 30: Completed Assembly (3 of 5)

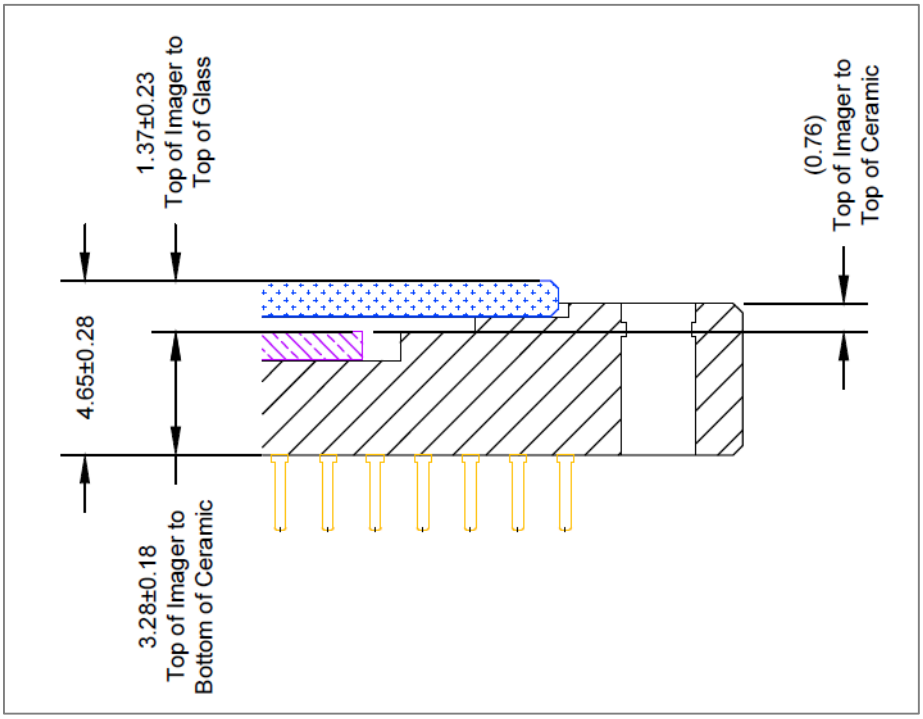


Figure 31: Completed Assembly (4 of 5)

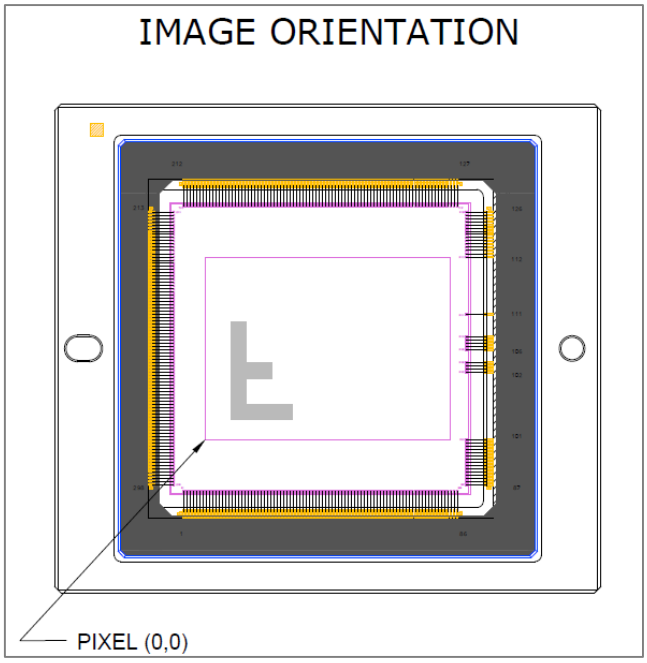
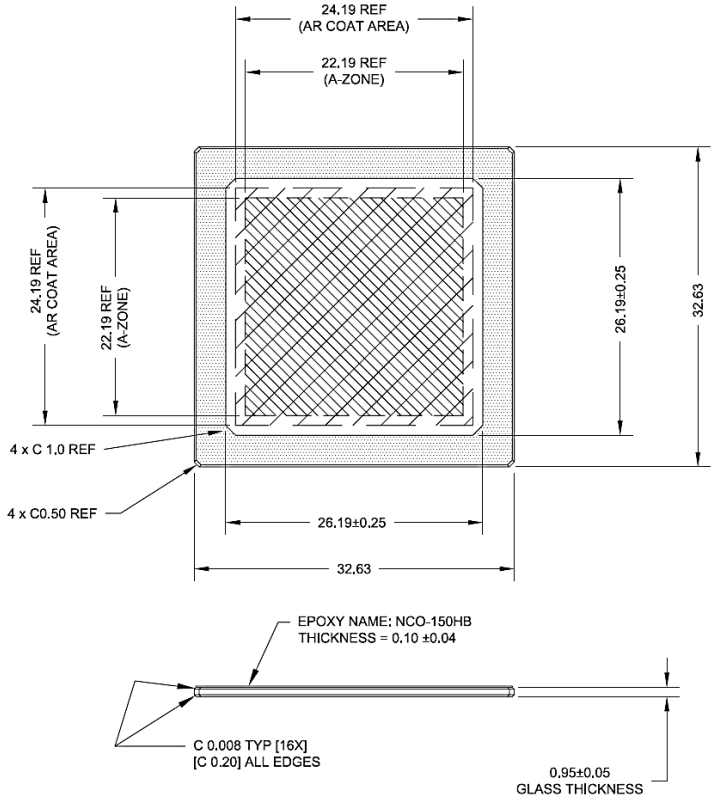


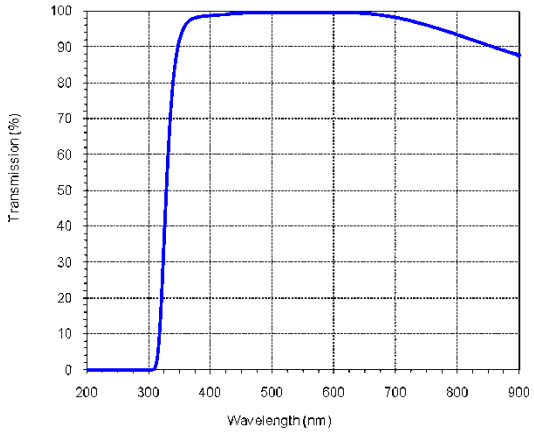
Figure 32: Completed Assembly (5 of 5)

MAR (Multi-layer AntiReflective coating) Cover Glass

Notes:

1. Units: IN [MM]
2. A-Zone Dust/Scratch Spec: 10 µm Maximum
3. Index of refraction: 1.5231





405-450 nm T > 98%
450-650 nm T > 99.%
650-690 nm T > 98%
690-770 nm T > 94%
770-870 nm T > 88%

Figure 33: MAR Cover Glass Specification

Quality Assurance and Reliability

Quality and Reliability

All image sensors conform to the specifications stated in this document. This is accomplished through a combination of statistical process control and visual inspection and electrical testing at key points of the manufacturing process, using industry standard methods. Information concerning the quality assurance and reliability testing procedures and results are available from ON Semiconductor upon request. For further information refer to Application Note *Quality and Reliability*.

Replacement

All devices are warranted against failure in accordance with the *Terms of Sale*. Devices that fail due to mechanical and electrical damage caused by the customer will not be replaced.

Liability of the Supplier

A reject is defined as an image sensor that does not meet all of the specifications in this document upon receipt by the customer. Product liability is limited to the cost of the defective item, as defined in the *Terms of Sale*.

Liability of the Customer

Damage from mishandling (scratches or breakage), electrostatic discharge (ESD), or other electrical misuse of the device beyond the stated operating or storage limits, which occurred after receipt of the sensor by the customer, shall be the responsibility of the customer.

Test Data Retention

Image sensors shall have an identifying number traceable to a test data file. Test data shall be kept for a period of 2 years after date of delivery.

Mechanical

The device assembly drawing is provided as a reference.

ON Semiconductor reserves the right to change any information contained herein without notice. All information furnished by ON Semiconductor is believed to be accurate.

Life Support Applications Policy

ON Semiconductor image sensors are not authorized for and should not be used within Life Support Systems without the specific written consent of ON Semiconductor.

Revision Changes

Revision Number	Description of Changes
1.0	• Initial Release
1.1	• Correction to Figure “Number of LVDS pairs (ports) used vs. bit depth”
1.2	• Correction to Figure “Number of LVDS pairs (ports) used vs. bit depth” • Update to the responsivity model and some specification values • Improved low temperature operating temperature specification • Update of register summary table
1.3	• Revised Clk In spec to be 45MHz -> 50 MHz • Updated branding

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5817−1050

ON Semiconductor Website: **www.onsemi.com**

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For additional information, please contact your local Sales Representative